

LITTLE FOOT®
Surface-Mount Power MOSFETs
Featured Products

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About LITTLE FOOT® Power MOSFETs

LITTLE FOOT power MOSFETs are being designed into computer and computer peripheral products, telecom systems, automotive air bags, and numerous other applications where space-savings and efficiency are at a premium. Built on high-density trench and planar technologies, LITTLE FOOT leads the industry for low-voltage, surface-mount power MOSFET performance.

TEMIC has expanded the scope of the LITTLE FOOT family beyond the classic SO-8 to include devices in the TSSOP-8*, and TSOP-6 packages, giving you even more genuine LITTLE FOOT options for your designs. Whether your application is load switching, power switching, dc-to-dc conversion, battery switching, or motor control, there's a LITTLE FOOT device that can help you reduce component count, save space, and use power more efficiently.

This publication includes complete data sheets for all the latest generations of LITTLE FOOT devices. To obtain data sheets for older members of the LITTLE FOOT family, please visit our web site at <http://www.temic.com>. Data sheets for all LITTLE FOOT products are also available from our faxback system using the document numbers provided in the LITTLE FOOT selector guide, which begins on page *i* of this data book.

About TEMIC Semiconductors

TEMIC Semiconductors is a division of TEMIC, a Daimler-Benz microelectronics company. Members of TEMIC Semiconductors include Siliconix, Telefunken Semiconductors, Matra MHS, and Dialog Semiconductors. With a rich technology portfolio including bipolar, CMOS, DMOS, silicon germanium and RF bipolar processes, TEMIC Semiconductors provides solutions that save space, prolong battery life, and reduce component count in pace-setting microelectronic designs.

* Formerly known as LITE FOOT®.

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Selector Guides

TSOP-6

TSOP-8

SOIC-8

Application Specific Standard MOSFETs (ASSAL)

Appendix

Worldwide Sales Offices and Distributors

TSOP-6 (N-Channel)

Part Number	Maximum Ratings					Page or FaxBack Number
	V _{DS} (V)	r _{DS(on)} (Ω)			I _D (A)	
		V _{GS} = 10 V	V _{GS} = 4.5 V	V _{GS} = 2.5 V		
Si3446DV	20		0.045	0.065	± 5.3	1-19
Si3442DV			0.070	0.095	± 4.0	1-11
Si3456DV	30	0.045	0.065		± 5.1	1-31
Si3454DV		0.065	0.095		± 4.2	1-23

TSOP-6 (P-Channel)

Part Number	Maximum Ratings					Page or FaxBack Number	
	V _{DS} (V)	r _{DS(on)} (Ω)					I _D (A)
		V _{GS} = 10 V	V _{GS} = 4.5 V	V _{GS} = 2.7 V	V _{GS} = 2.5 V		
Si3443DV	-20		0.065	0.090	0.100	± 4.4	1-15
Si3441DV			0.100		0.135	± 3.3	1-7
Si3455DV	-30	0.100	0.190			± 3.5	1-27
Si3457DV		0.065	0.100			± 4.2	1-35

TSSOP-8 (N-Channel)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V _{DS} (V)	r _{DS(on)} (Ω)				I _D (A)		
		V _{GS} = 10 V	V _{GS} = 4.5 V	V _{GS} = 3.0 V	V _{GS} = 2.5 V			
Si6466DQ	20		0.014		0.021	± 7.8	Single	2-33
Si6968DQ			0.022		0.030	± 6.5	Dual	2-101
Si6426DQ			0.035		0.040	± 5.4	Single	2-9
Si6966DQ			0.035		0.050	± 4.5	Dual	2-97
Si6926DQ			0.035	0.040	0.045	± 4.0	Dual	2-65
Si6925DQ			0.050	0.060	0.080	± 3.4	Dual	2-61
Si6946DQ			0.080		0.110	± 2.8	Dual	2-81
Si6410DQ	30	0.014	0.021			± 7.8	Single	2-1
Si6434DQ		0.028	0.042			± 5.6	Single	2-17
Si6928DQ		0.035	0.050			± 4.0	Dual	2-69
Si6954DQ		0.065	0.095			± 3.9	Dual	2-85

Note

- a. The data sheet for this product has not been included in this publication. It is available on the TEMIC web site (<http://www.TEMIC.com>) or via facsimile by calling Siliconix FaxBack, 1-408-970-5600 and requesting the FaxBack document number indicated.

TSSOP-8 (P-Channel)

Part Number	Maximum Ratings				Config.	Page or FaxBack Number	
	V _{DS} (V)	r _{DS(on)} (Ω)					I _D (A)
		V _{GS} = -10 V	V _{GS} = -4.5 V	V _{GS} = -2.5 V			
Si6433DQ	-12		0.060	0.090	± 4.0	Single	2-13
Si6943DQ			0.100	0.180	± 2.5	Dual	2-77
Si6463DQ	-20		0.020	0.030	± 6.5	Single	2-29
Si6963DQ			0.050	0.085	± 3.5	Dual	2-93
Si6953DQ		0.170	0.320		± 1.9	Dual	70170 ^a
Si6415DQ	-30	0.019	0.030		± 6.5	Single	2-5
Si6435DQ		0.040	0.070		± 4.5	Single	2-21
Si6933DQ		0.045	0.085		± 3.5	Dual	2-73
Si6955DQ		0.085	0.190		± 2.5	Dual	2-89
Si6459DQ		-60	0.120	0.150		± 2.6	Single

TSSOP-8 (Complementary Devices)

Part Number	Maximum Ratings					Config.	Page or FaxBack Number
	V _{DS} (V)	r _{DS(on)} (Ω)			I _D (A)		
		V _{GS} = ± 10 V	V _{GS} = ± 4.5 V	V _{GS} = ± 2.5 V			
Si6552DQ	20 -12		0.080 0.100	0.110 0.180	± 2.8 ± 2.5	N-Channel P-Channel	2-49
Si6562DQ	20 -20		0.035 0.045	0.050 0.085	± 4.5 ± 3.5	N-Channel P-Channel	2-55
Si6544DQ	30 -30	0.035 0.045	0.050 0.090		± 4.0 ± 3.4	N-Channel P-Channel	2-43
Si6543DQ		0.065 0.085	0.095 0.190		± 3.9 ± 2.5	N-Channel P-Channel	2-37

8-Pin SOIC (N-Channel)

Part Number	Maximum Ratings					Config.	Page or FaxBack Number	
	V _{DS} (V)	r _{DS(on)} (Ω)						I _D (A)
		V _{GS} = 10 V	V _{GS} = 6.0 V	V _{GS} = 4.5 V	V _{GS} = 2.5 V			
Si9426DY	20			0.0135	0.016	± 10	Single	70160 ^a
Si4966DY				0.025	0.035	± 7.1	Dual	3-89
Si9926DY				0.030	0.040	± 6.0	Dual	70162 ^a
Si4466DY				0.009	0.013	± 13.2	Single	3-29
Si9956DY		0.100		0.200		± 3.5	Dual	70140 ^a
Si4420DY	30	0.009		0.013		± 12.5	Single	3-9
Si4920DY				0.025	0.035	± 6.9	Dual	3-65
Si4410DY		0.0135		0.020		± 10	Single	3-1
Si4416DY		0.018		0.028		± 9.0	Single	3-5

Note

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8-Pin SOIC (N-Channel)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V _{DS} (V)	r _{DS(on)} (Ω)				I _D (A)		
		V _{GS} = 10 V	V _{GS} = 6.0 V	V _{GS} = 4.5 V	V _{GS} = 2.5 V			
Si4412DY	30	0.028		0.042		± 7.0	Single	70154 ^a
Si9410DY		0.030		0.050		± 7.0	Single	70122 ^a
Si4936DY		0.037		0.055		± 5.8	Dual	3-73
Si9936DY		0.050		0.080		± 5.0	Dual	70128 ^a
Si4450DY	60	0.024	0.030			± 7.5	Single	3-21
Si4946EY		0.055		0.075		± 4.5	Dual	3-77
Si9945AEY		0.080		0.100		± 3.7	Dual	70758 ^a
Si4480DY	80	0.035	0.040			± 6.0	Single	3-33
Si4980DY		0.075	0.095			± 3.7	Dual	3-93
Si4482DY	100	0.060	0.080			± 4.6	Single	3-37
Si4982DY		0.150	0.180			± 2.6	Dual	3-97

8-Pin SOIC (P-Channel)

Part Number	Maximum Ratings							Page or FaxBack Number
	V _{DS} (V)	r _{DS(on)} (Ω)				I _D (A)		
		V _{GS} = -10 V	V _{GS} = -4.5 V	V _{GS} = -2.7 V	V _{GS} = -2.5 V			
Si9434DY	-12		0.040		0.060	± 6.4	Single	70147 ^a
Si9934DY			0.050		0.074	± 5.0	Dual	70163 ^a
Si4463DY	-20		0.014		0.020	± 10.0	Single	3-25
Si9424DY			0.025		0.033	± 7.7	Single	3-101
Si4963DY			0.033		0.050	± 6.2	Dual	3-85
Si9433DY			0.065		0.100	± 5.4	Single	70125 ^a
Si9933ADY			0.075	0.115		± 3.4	Dual	70651 ^a
Si9430DY		0.050	0.090			± 5.8	Single	70124 ^a
Si9400DY		0.250	0.400			± 2.5	Single	70119 ^a
Si9953DY		0.250	0.400			± 2.3	Dual	70138 ^a
Si4425DY		0.014	0.023			± 11	Single	3-13
Si4925DY		0.032	0.045			± 6.1	Dual	3-69
Si4435DY	-30	0.020	0.035			± 8.0	Single	3-17
Si4431DY		0.040	0.070			± 5.8	Single	70151 ^a
Si4953DY		0.053	0.095			± 4.9	Dual	70153 ^a
Si9435DY		0.055	0.105			± 5.1	Single	70126 ^a
Si4947DY		0.085	0.190			± 3.5	Dual	70156 ^a
Si4948EY		0.120	0.150			± 3.1	Dual	3-81
Si9407AEY	-60	0.120	0.150			± 3.5	Single	70742 ^a
Si9948AEY		0.170	0.260			± 2.6	Dual	70759 ^a

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8-Pin SOIC (Complementary Devices)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V _{DS} (V)	r _{DS(on)} (Ω)				I _D (A)		
		V _{GS} = ± 10 V	V _{GS} = ± 4.5 V	V _{GS} = ± 2.7 V	V _{GS} = ± 2.5 V			
Si4562DY	20 -20		0.025 0.033		0.035 0.050	± 7.1 ± 6.0	N-Channel P-Channel	3-59
Si9942DY		0.125 0.200	0.250 0.350			± 3.0 ± 2.5	N-Channel P-Channel	70130 ^a
Si4542DY	30 -30	0.025 0.032	0.035 0.045			± 6.9 ± 6.1	N-Channel P-Channel	3-47
Si4539DY		0.037 0.053	0.055 0.095			± 5.8 ± 4.9	N-Channel P-Channel	70152 ^a
Si9939DY		0.050 0.100	0.080 0.160			± 3.5 ± 3.5	N-Channel P-Channel	70146 ^a
Si4532DY		0.065 0.085	0.095 0.190			± 3.9 ± 3.1	N-Channel P-Channel	3-41
Si4559EY	60 -60	0.055 0.120	0.075 0.150			± 4.5 ± 3.1	N-Channel P-Channel	3-53

Application-Specific Standard MOSFETs (ASSM)

Part Number	Maximum Ratings					Config.	Package	Page or FaxBack Number
	V _{DS} (V)	r _{DS(on)} (Ω)			I _D (A)			
		V _{GS} = 10 V	V _{GS} = 4.5 V	V _{GS} = 3.0 V				
Dual Gate, High-Efficiency, PWM MOSFETS								
Si4806DY	30	0.022	0.030		± 7.7 ± 2.0	Dual Gate N-Channel	SOIC-8	4-3
Si4807DY	-30	0.035	0.054		± 6.0 ± 0.9	Dual Gate P-Channel	SOIC-8	4-8
High-Efficiency, PWM Optimized MOSFETs								
Si9804DY	20		0.023	0.030	± 7.8	Single N-Channel	SOIC-8	4-45
Si9803DY	-20		0.040	0.060	± 5.9	Single P-Channel	SOIC-8	4-41
Si9802DY	20		0.055	0.075	± 4.5	Dual N-Channel	SOIC-8	4-37
Si9801DY	20 -20		0.055 0.080	0.075 0.120	± 4.5 ± 4.0	N-Channel P-Channel	SOIC-8	4-31
Si6802DQ	20		0.075	0.110	± 3.3	Single N-Channel	TSSOP-8	4-21
Si6803DQ	20 -20		0.095 0.110	0.145 0.165	± 2.5 ± 2.3	N-Channel P-Channel	TSSOP-8	4-25
Si6801DQ	20 -20		0.160 0.190	0.260 0.280	± 1.9 ± 1.7	N-Channel P-Channel	TSSOP-8	4-15

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Selector Guides

TSOP-6

1

TSSOP-8

SOIC-8

Application Specific Standard MOSFETs (ASSM)

Appendix

Worldwide Sales Offices and Distributors

TSOP-6—The Next Step for LITTLE FOOT®

Cellular telephones, notebook computers, and other portable electronic systems are becoming smaller with each new generation of products. The new TSOP-6 LITTLE FOOT family anticipates this evolution. Its small size allows the placement of a MOSFET in spaces that have become too small for any other surface-mount power MOSFET package.

With a power rating of 2 W, on-resistance as low as 0.065Ω , and current ratings of up to 4.2 A, the new LITTLE FOOT TSOP-6 (Figure 1) is a true power package, providing the kind of performance, on an even smaller scale, that designers have come to expect from LITTLE FOOT.

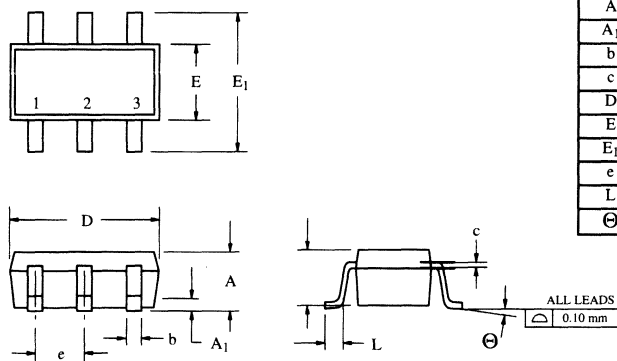


Figure 1. TSOP-6 Outline Drawing

Not only is the TSOP-6 small, it's also a JEDEC-registered package [with the same footprint as the SC-59, but with a lower profile and higher power rating (up to 2 W)]. As further assurance that the TSOP-6 will be established as the industry standard for low-voltage applications with limited circuit board space, these devices are being second-sourced by Motorola Semiconductors. For these TSOP-6 devices, Siliconix and Motorola have agreed on compatible pin-outs, power ratings, and package outlines and dimensions.

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	—	1.10	—	0.043
A ₁	0.01	0.10	0.0004	0.004
b	0.25	0.50	0.010	0.020
c	0.10	0.26	0.004	0.010
D	2.90	3.10	0.114	0.122
E	1.30	1.70	0.051	0.067
E ₁	2.75 BSC		0.108 BSC	
e	1.00 BSC		0.039 BSC	
L	0.20	0.60	0.008	0.024
Θ	0°	8°	0°	8°

TSOP-6

1

A New Branch of a Great Family

When Siliconix created the first true surface-mount power MOSFETs with its SO-8 LITTLE FOOT family, two innovations were involved: a lower on-resistance power MOSFET technology and modifications to the standard, surface-mount SOIC package. The lower on-resistance MOSFET reduced the power dissipation per unit of current, while the innovative packaging provided a path for heat to escape, allowing high currents to be switched in a package that is much smaller and easier to assemble.

The introduction of LITTLE FOOT MOSFETs in the SO-8 inevitably raised the expectations of the market regarding surface-mounted power MOSFETs, resulting in a demand for devices with greater capabilities in even smaller packages. In 1994, Siliconix halved the size of the smallest available power MOSFET package with the introduction of the LITTLE FOOT TSSOP-8.

With the introduction of LITTLE FOOT devices in the TSOP-6, Siliconix is answering the demand of the market for smaller size and greater capabilities with even smaller devices that can provide the current handling available, until now, only in the TSSOP-8, SO-8, and other larger packages.

The Footprint

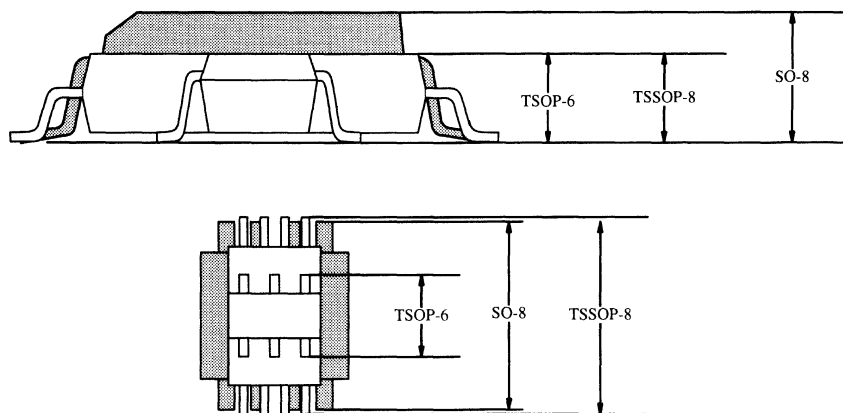


Figure 2. LITTLE FOOT® Family Package Evolution

The TSOP-6 is a 6-leaded, 1-mm thick package with a total height of 1.1 mm. The package and leads occupy an area of 2.75×3.10 mm. To put this in perspective, Figure 2 gives a visual comparison by overlaying the package outlines of the TSOP-6, the TSSOP-8, and the SO-8 packages. The TSOP-6 measures 2.75 mm in width including the leads, less than half as wide as the SO-8. Table 1 gives a comparison of the dimensions of these packages.

Table 1. Comparison of Dimensions

Dim	TSOP-6				TSSOP-8				SOIC-8			
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Height	—	1.10	—	0.043	1.05	1.20	0.041	0.047	1.35	1.75	0.053	0.069
Lead Width	0.25	0.50	0.010	0.020	0.25	0.30	0.010	0.012	0.35	0.45	0.014	0.018
Package Length	2.90	3.10	0.114	0.122	2.90	3.10	0.114	0.122	4.69	5.00	0.185	0.196
Package Width	1.30	1.70	0.051	0.067	4.30	4.50	0.170	0.177	3.50	4.05	0.140	0.160
Width of Foot Print	2.75 BSC		0.108 BSC		6.20	6.60	0.244	0.260	5.70	6.30	0.224	0.248
Lead Pitch	1.00 BSC		0.039 BSC		0.65 BSC		0.025 BSC		1.27 BSC		0.050 BSC	

Thermal Capabilities

The same copper lead frame innovations introduced in the SO-8 LITTLE FOOT have been used in the TSOP-6 LITTLE FOOT to dissipate heat. The TSOP-6 lead frame is shown in Figure 3. As in the SO-8 and TSSOP-8 packages, the thermal path runs from the die, through the die attach, into the copper lead frame, and out the drain leads (Figure 4). The drain leads account for the largest portion of the thermal impedance due to the small cross sectional area of the leads. The small size of the package helps to keep the length of the drain leads short. The short lead length, in combination with the use of four drain leads, keeps the thermal impedance low for this size package.

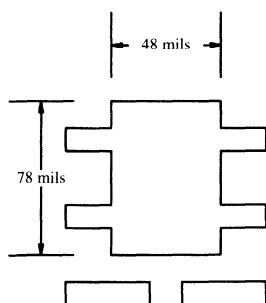


Figure 3. TSOP-6 Leadframe

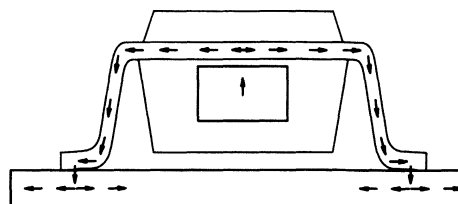


Figure 4. Thermal Path

The thermal rating provided on data sheets for surface-mount MOSFETs is measured with the part mounted on a one-inch square piece of 0.062-inch thick FR4 PC board. This choice of test board is neither a “worst-case” or “best-case” layout. It represents a compromise between single-layer and multilayer boards, with more copper on its single side than the average single-layer construction. Thus, it can serve as an approximation of multilayer boards with center power planes and far less surface copper.

The junction is heated by a known amount of power for a known amount of time. The junction temperature is measured immediately after heating using the temperature coefficient of the forward voltage of the internal diode. This procedure is repeated from a time of 5 ms out to several hundred seconds. This series of measurements and measurement of the ambient temperature provides $R\theta_{ja}$, the single pulse power curve, and provides the data required to generate the transient thermal impedance curves from junction to ambient.

Two Versions: 0.5 W and 2 W

Each TSOP-6 LITTLE FOOT device is available in two versions with different thermal ratings. The rating is dependent on the lead frame material used. The parts with the "V" suffix are built with a copper leadframe which gives the best thermal performance. The parts with the "X" suffix have an Alloy 42 leadframe. Although the "X" series devices are rated with the same electrical resistance as the "V" series devices, they are specified at a reduced current level to compensate for their increased thermal impedance.*

The first thermal performance parameter that is normally seen is $R\theta_{ja}$. This parameter gives a means of comparing the package capability before the PC board starts to have a significant effect. For the TSOP-6, the board is considered to dominate after 5 seconds. $R\theta_{ja}$ for the TSOP-6 is 62.5°C/W for the "V" parts and 90°C/W for the "X" parts. The "V" parts, which have the copper lead frame, compare very favorably with 50°C/W for the single-die SO-8, 62.5°C/W for the dual-die SO-8.

A comparison of the single-pulse power curves (Figure 5) reveals the difference in the thermal mass of the TSOP-6 and the SO-8 die and lead frames and therefore in ability of these two packages to handle surge currents. The single-pulse power curve shows the amount of power it takes for a single pulse of fixed duration to raise the junction temperature from room temperature to 150°C . If extended below 10 ms, the curves would become asymptotic and converge, reflecting the limitations of the die alone. The opposite end of the curve reflects the limitations of the PC board upon which the device is mounted. The difference in thermal mass shows up in between. The reduced thermal mass of the TSOP-6 results in a significant but reduced capability in pulse duration, amounting to less than 5 seconds. It should be noted that the TSOP-6 can dissipate a 30-W pulse of 10-ms duration.

Samples of "X"-series devices will be available in Q1, 1998. Please contact us at 1-800-554-5565 (1-408-567-8220 outside the U.S. and Canada) to receive data sheets for these devices.

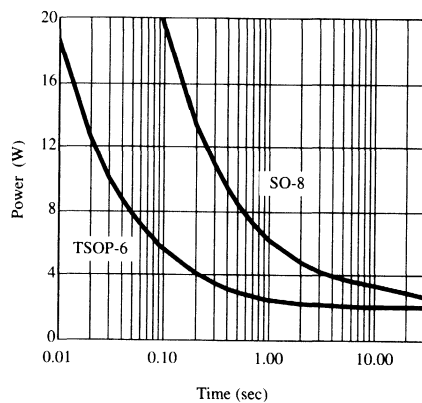


Figure 5. Single Pulse Power

The combination of very low on-resistance power MOSFET technology and a thermally efficient copper leadframe in the new LITTLE FOOT TSOP-6 package creates a new standard for performance per footprint. For applications requiring very low on-resistance at less current, the Alloy 42-leadframes offer manufacturing advantages that make them even more economical.

1

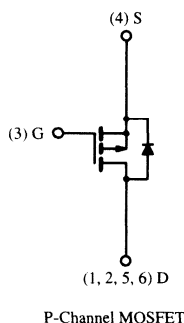
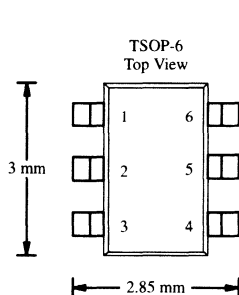
TSOP-6

P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.10 @ $V_{GS} = -4.5$ V	± 3.3
	0.135 @ $V_{GS} = -2.5$ V	± 2.9

2.5-V Rated



Power Dissipation
Si3441DV—2.0 W

1
TSOP-6

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 3.3	A
	$T_A = 70^\circ\text{C}$		± 2.6	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a		I_S	-1.6	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.0	W
	$T_A = 70^\circ\text{C}$		1.28	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70191.

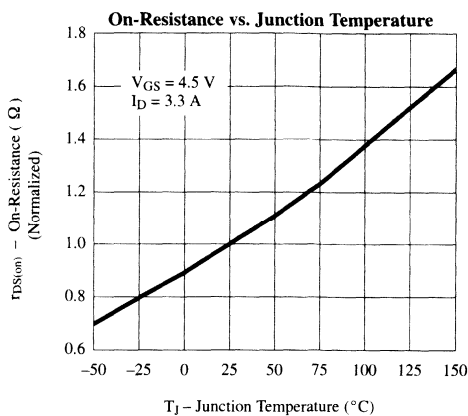
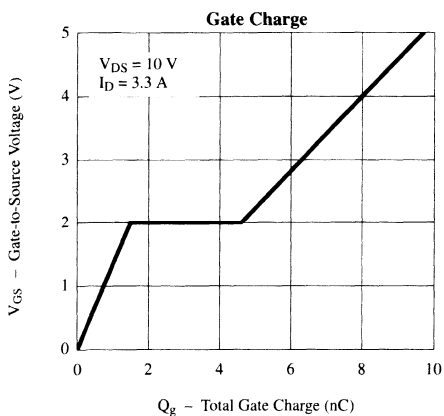
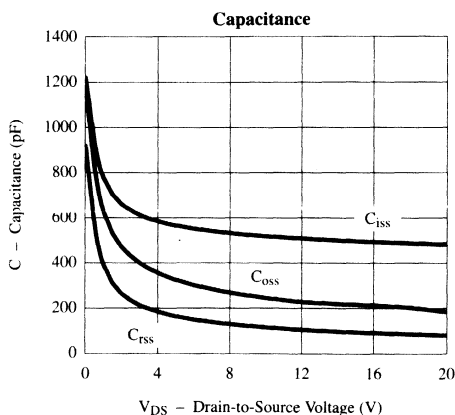
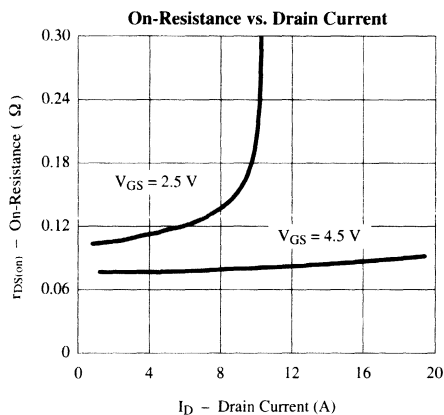
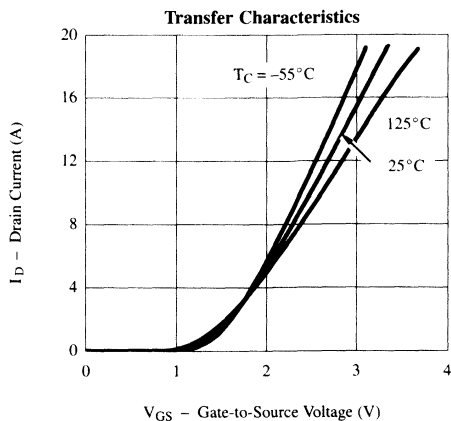
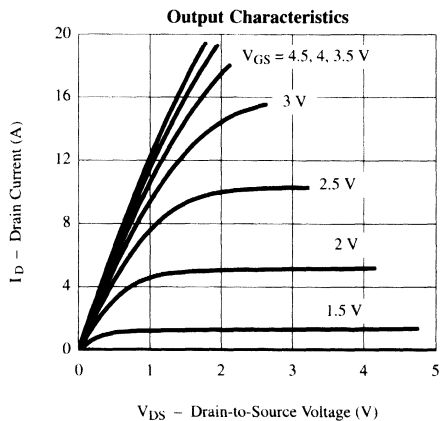
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-0.45			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-10			A
		$V_{DS} = -5\ \text{V}, V_{GS} = -2.5\ \text{V}$	-4			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = 3.3\ \text{A}$		0.078	0.10	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = 2.9\ \text{A}$		0.110	0.135	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -3.3\ \text{A}$		8.8		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.6\ \text{A}, V_{GS} = 0\ \text{V}$		0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -3.3\ \text{A}$		8.6	14	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			3.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1.6\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		27	50	ns
Rise Time	t_r			17	30	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			45	70	
Source-Drain Reverse Recovery Time	t_{rr}			50	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

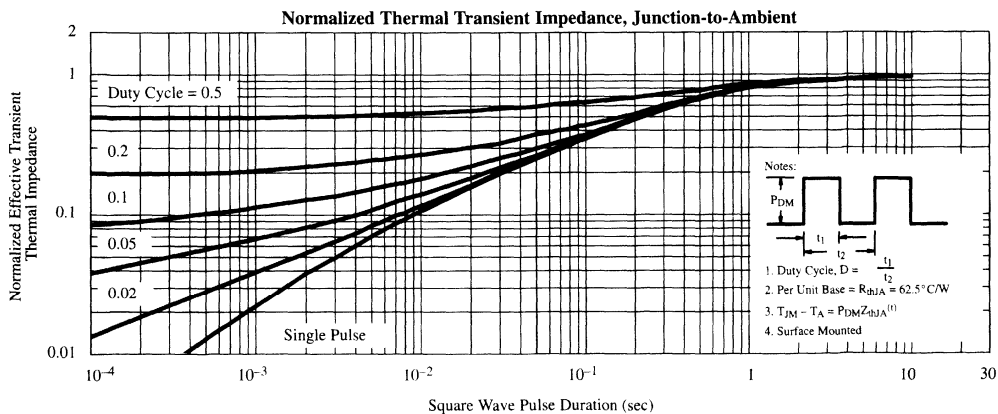
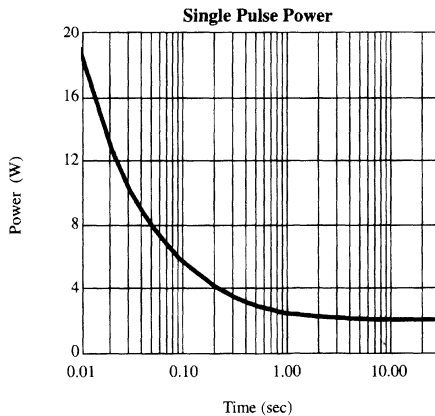
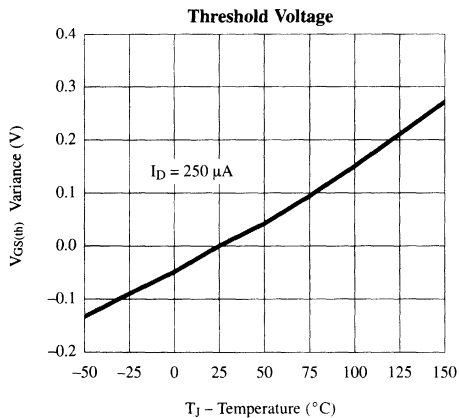
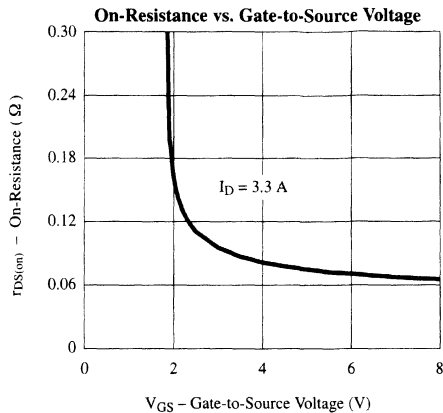
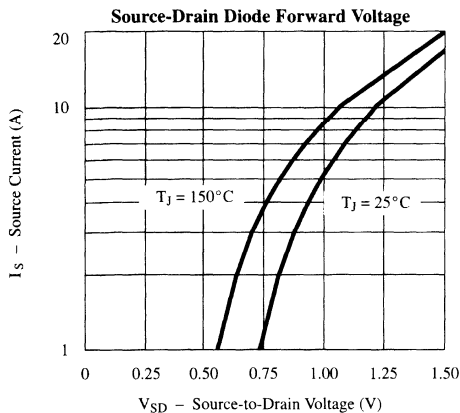
Typical Characteristics (25°C Unless Otherwise Noted)



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TSOP-6

Typical Characteristics (25°C Unless Otherwise Noted)

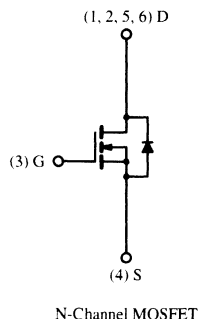
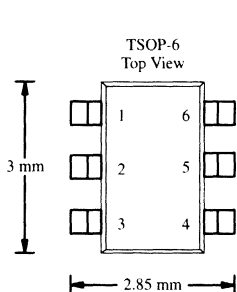


N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.07 @ V _{GS} = 4.5 V	± 4.0
	0.095 @ V _{GS} = 2.5 V	± 3.4

2.5-V Rated



Power Dissipation
Si3442DV—2.0 W

1
TSOP-6

Absolute Maximum Ratings (T_A = 25° C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	± 20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150° C) ^a	I _D	± 4.0	A
		± 3.1	
Pulsed Drain Current	I _{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I _S	± 1.6	
Maximum Power Dissipation ^a	P _D	2.0	W
		1.28	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 5 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70192.

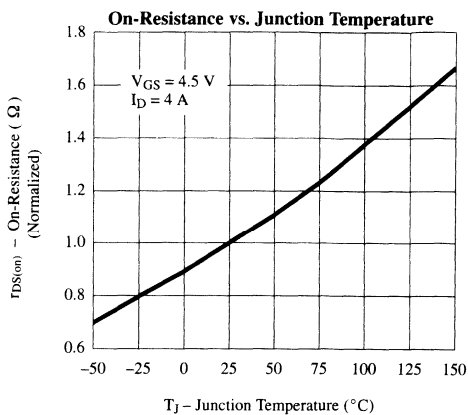
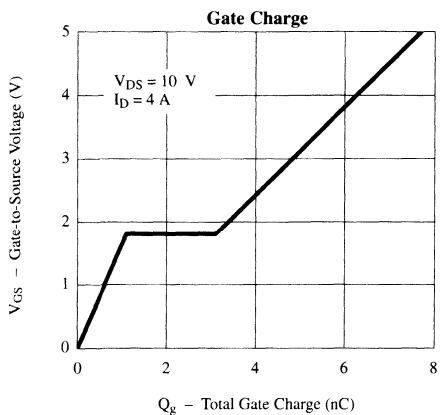
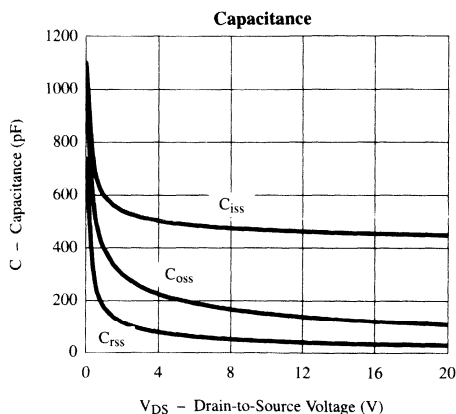
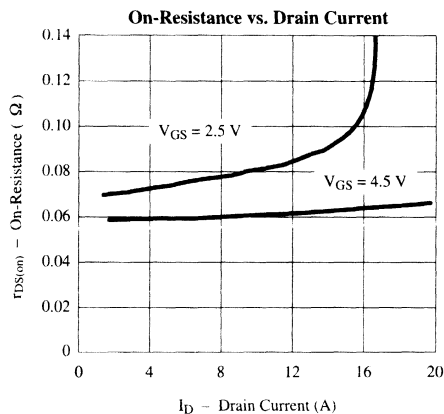
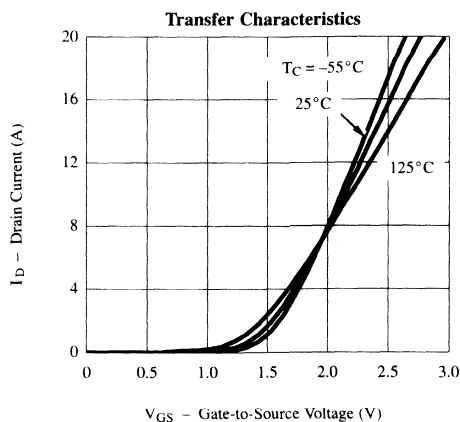
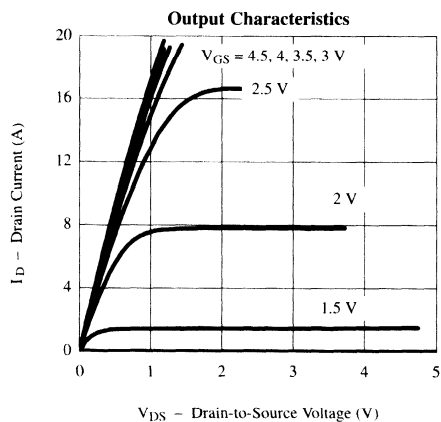
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	10			A
On-State Drain Current ^a		$V_{DS} = 5\ \text{V}, V_{GS} = 2.5\ \text{V}$	4			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 4.0\ \text{A}$		0.058	0.07	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 3.4\ \text{A}$		0.072	0.095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 4.0\ \text{A}$		11.3		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.6\ \text{A}, V_{GS} = 0\ \text{V}$		0.75	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 4.0\ \text{A}$		7.0	10	nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			2.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		8	20	ns
Rise Time	t_r			24	40	
Turn-Off Delay Time	$t_{d(off)}$			35	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.6\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		40	70	

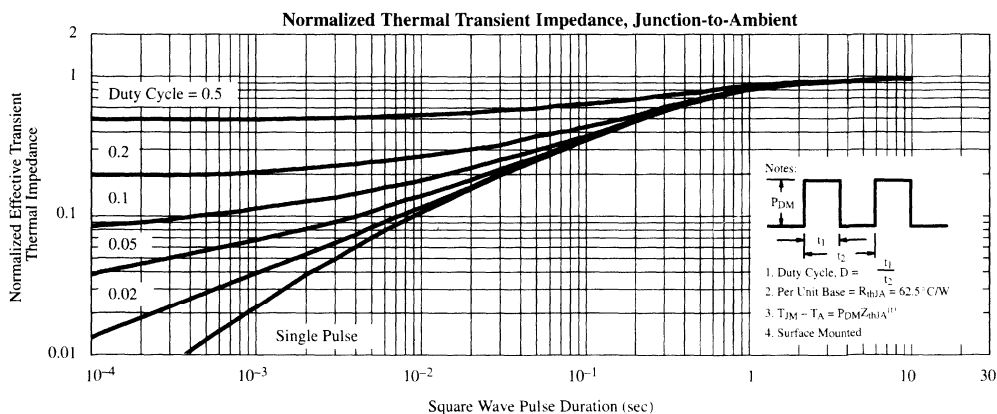
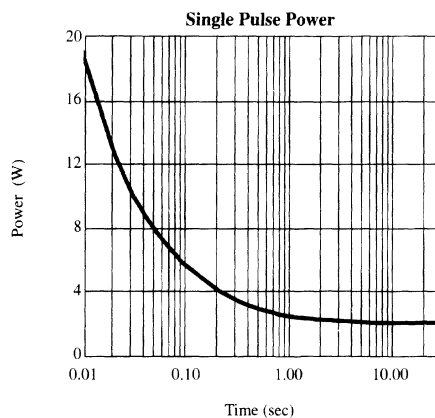
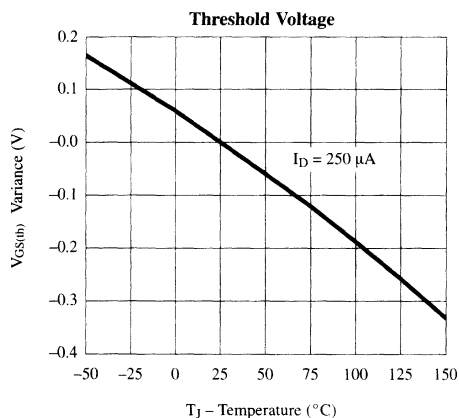
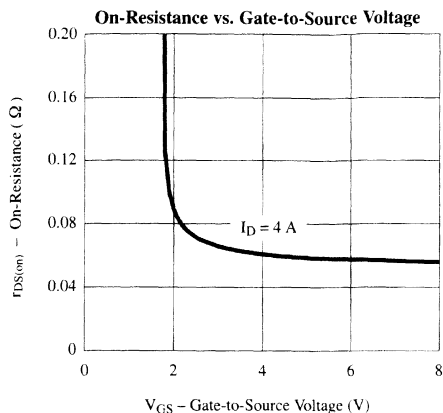
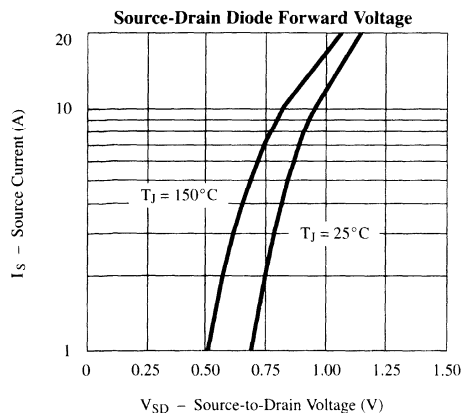
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

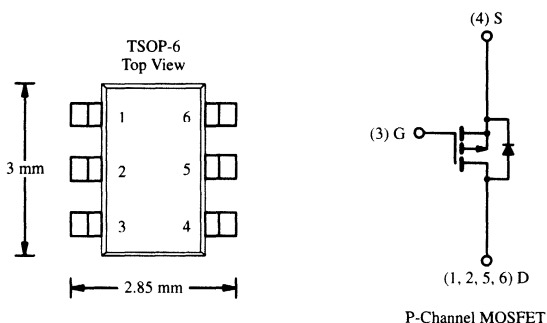


P-Channel, 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.065 @ $V_{GS} = -4.5$ V	± 4.4
	0.090 @ $V_{GS} = -2.7$ V	± 3.7
	0.100 @ $V_{GS} = -2.5$ V	± 3.5

TrenchFET™
Power MOSFETs
2.5-V Rated



1

TSOP-6

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	A
	$T_A = 70^\circ\text{C}$	± 4.4	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	W
	$T_A = 70^\circ\text{C}$	2.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70713.

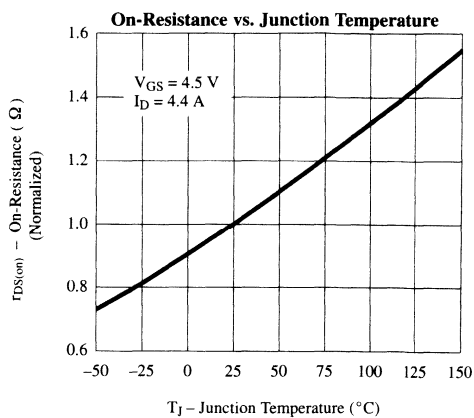
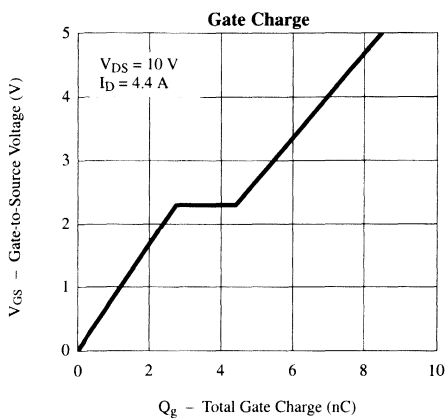
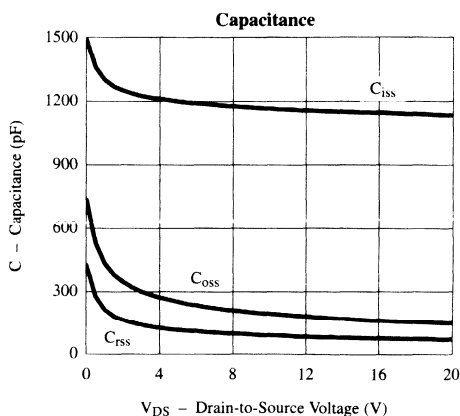
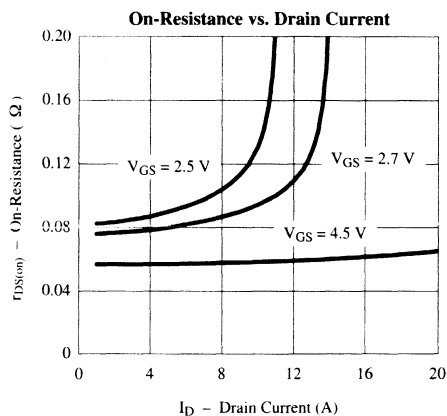
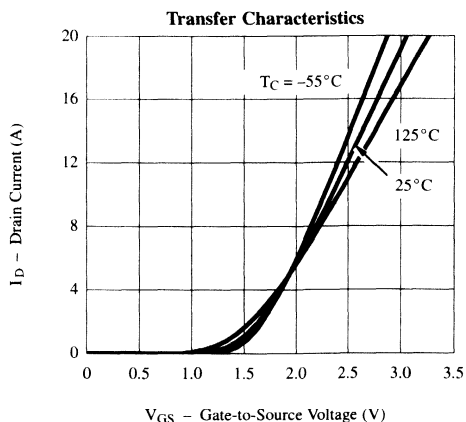
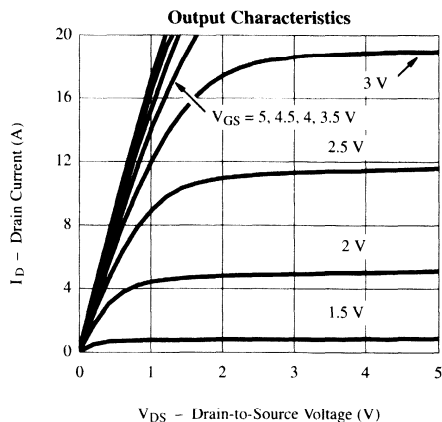
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -4.4\ \text{A}$		0.058	0.065	Ω
		$V_{GS} = -2.7\ \text{V}, I_D = -3.7\ \text{A}$		0.080	0.090	
		$V_{GS} = -2.5\ \text{V}, I_D = -3.5\ \text{A}$		0.087	0.100	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -4.4\ \text{A}$		10		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.7\ \text{A}, V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -4.4\ \text{A}$		8.5	15	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			1.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \approx -1.0\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		15	50	ns
Rise Time	t_r			32	60	
Turn-Off Delay Time	$t_{d(off)}$			57	100	
Fall Time	t_f			40	80	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		40	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

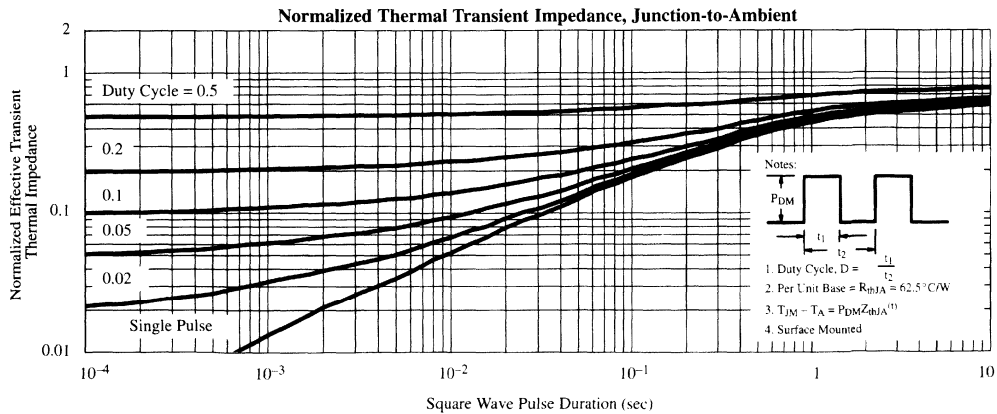
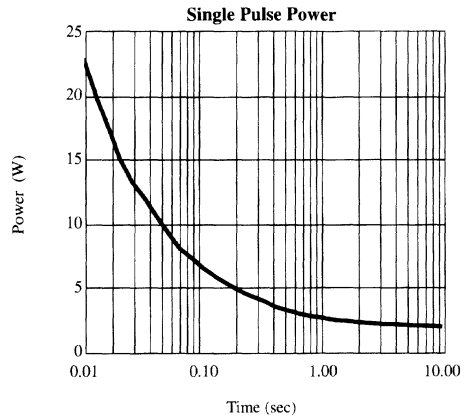
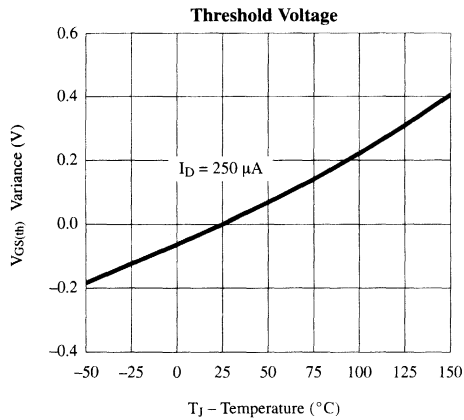
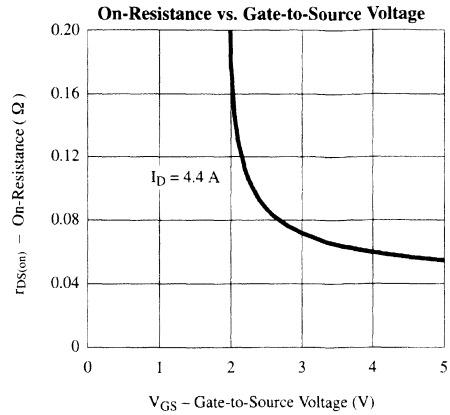
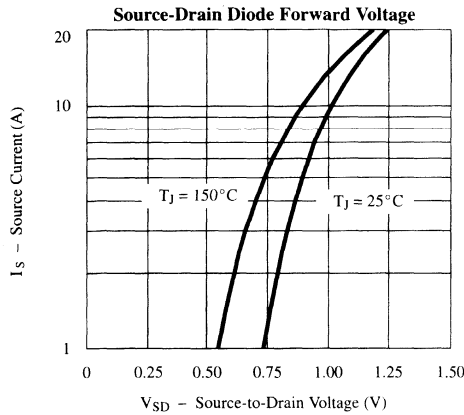
Typical Characteristics (25°C Unless Otherwise Noted)



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TSOP-6

Typical Characteristics (25°C Unless Otherwise Noted)

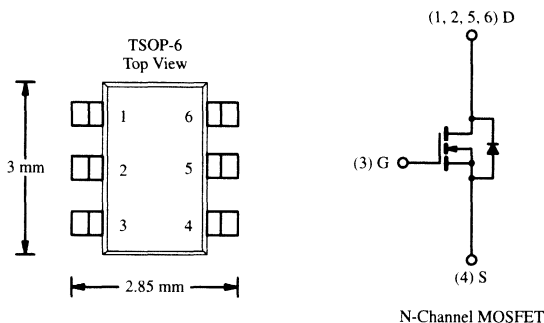


N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.045 @ $V_{GS} = 4.5$ V	± 5.3
	0.065 @ $V_{GS} = 2.5$ V	± 4.4

TrenchFET™
Power MOSFETs
2.5-V Rated



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TSOP-6

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	± 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 5.3	A
		± 4.2	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	± 1.7	
Maximum Power Dissipation ^a	P_D	2.0	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70715.

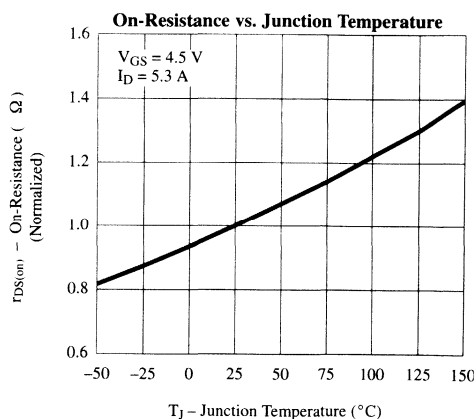
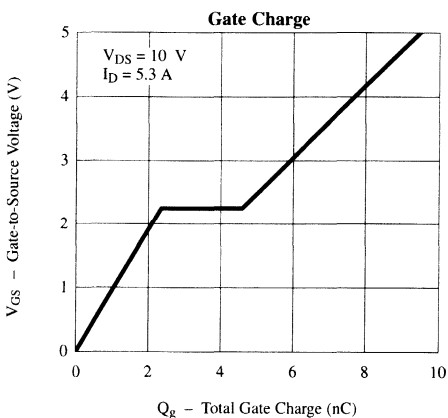
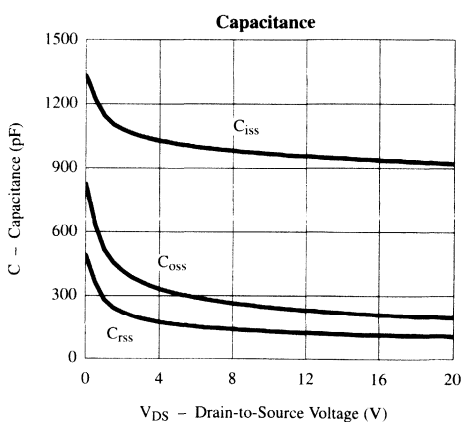
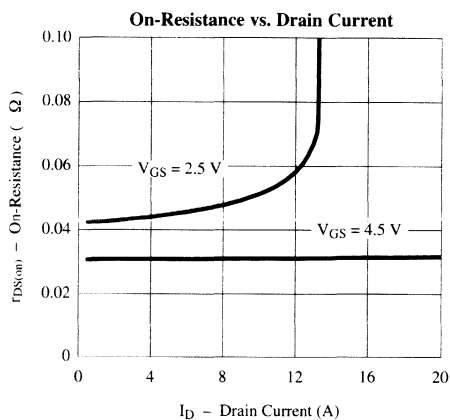
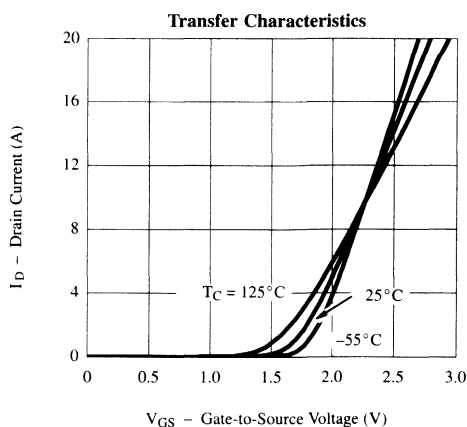
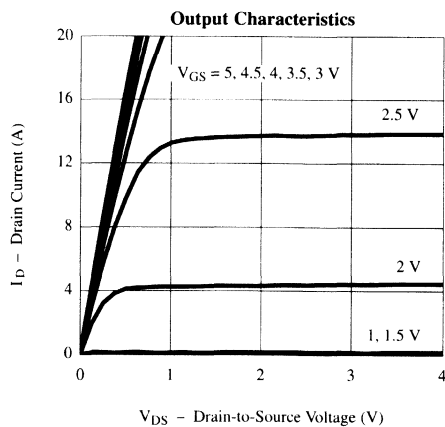
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	10			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 5.3\ \text{A}$		0.032	0.045	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 4.4\ \text{A}$		0.045	0.065	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 5.3\ \text{A}$		20		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 5.3\ \text{A}$		10	20	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		30	50	ns
Rise Time	t_r			50	80	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			35	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	90	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

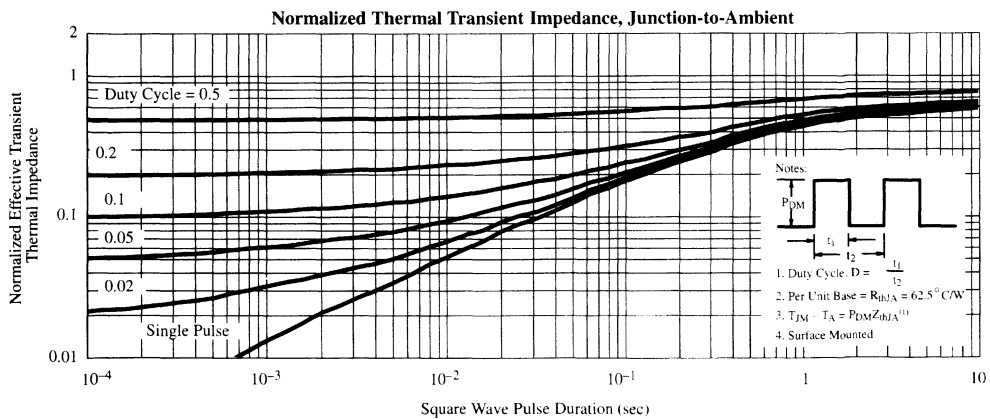
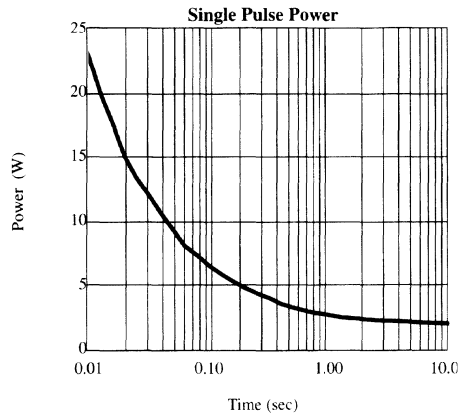
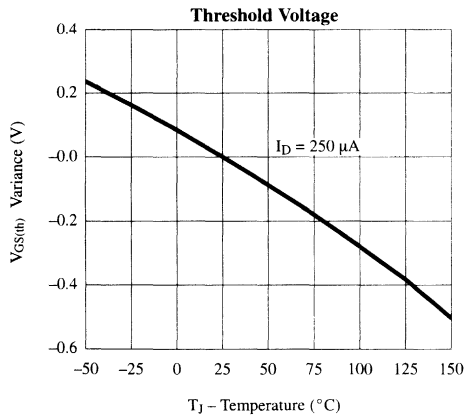
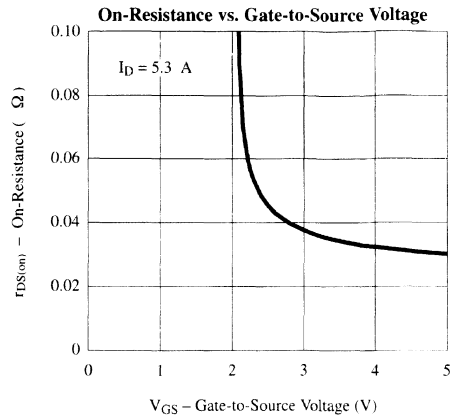
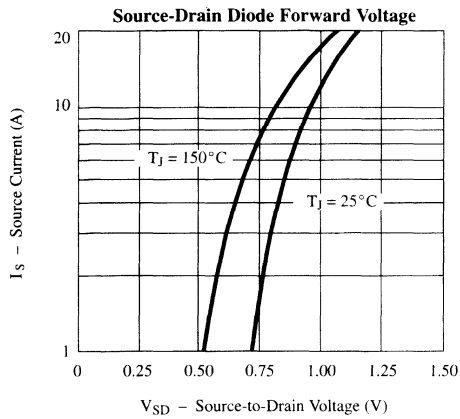
Typical Characteristics (25°C Unless Otherwise Noted)



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Typical Characteristics (25°C Unless Otherwise Noted)

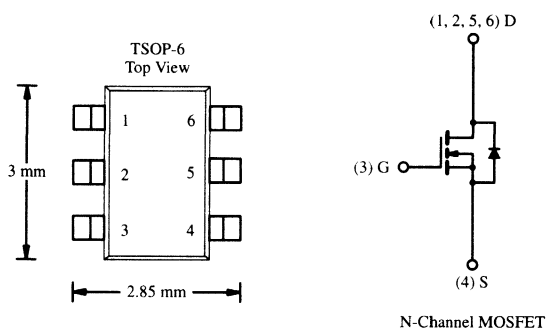


N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.065 @ $V_{GS} = 10$ V	± 4.2
	0.095 @ $V_{GS} = 4.5$ V	± 3.4

TrenchFET™
Power MOSFETs



Power Dissipation
Si3454DV—2.0 W

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TSOP-6

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	± 30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 4.2	A
		± 3.4	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	± 1.7	
Maximum Power Dissipation ^a	P_D	2.0	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70193. A SPICE Model data sheet is available for this product (FaxBack document #70637).

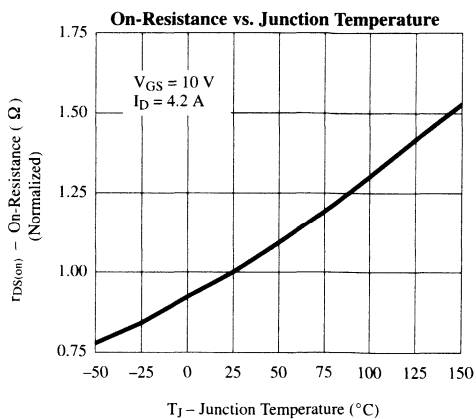
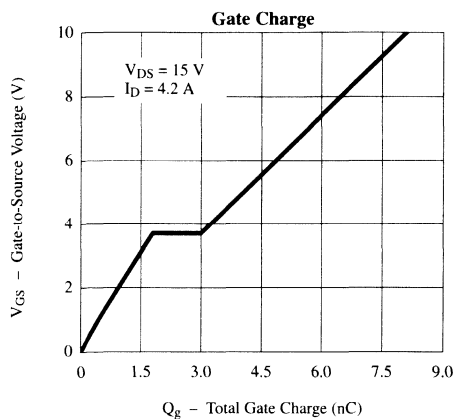
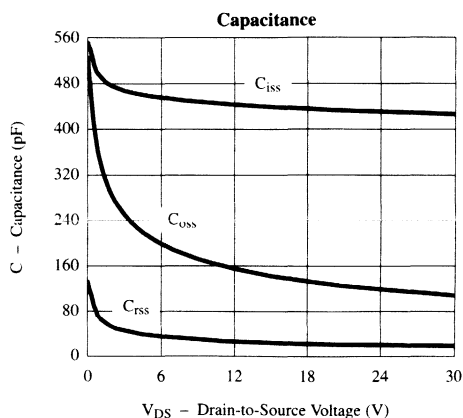
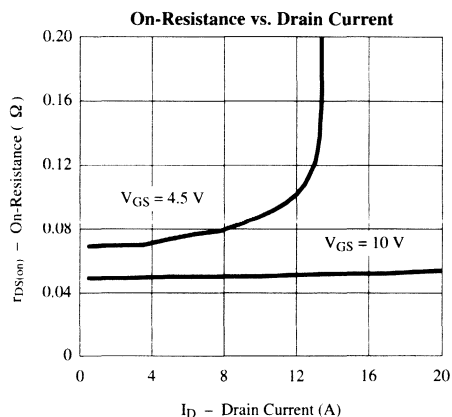
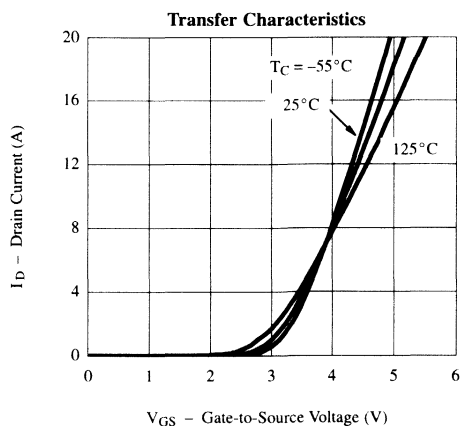
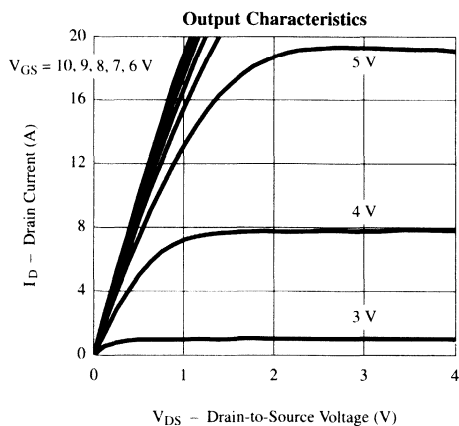
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 4.2\ \text{A}$		0.050	0.065	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 3.4\ \text{A}$		0.070	0.095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 4.2\ \text{A}$		7		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 4.2\ \text{A}$		8	15	nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \equiv 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			20	35	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

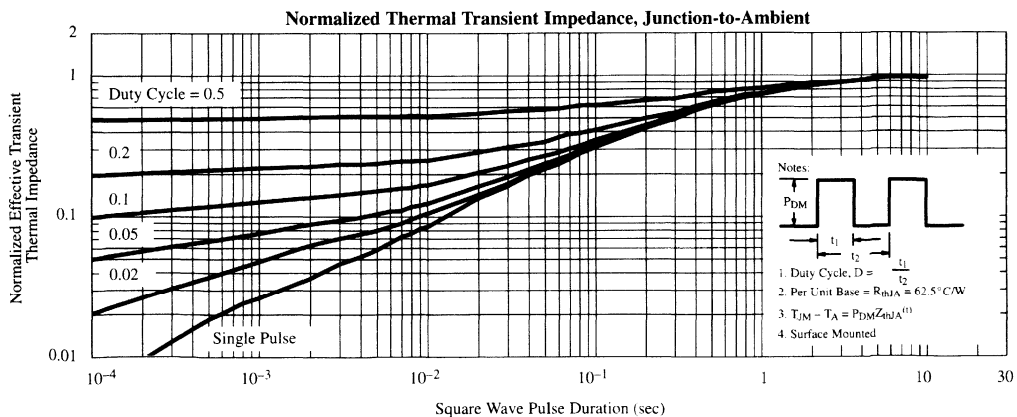
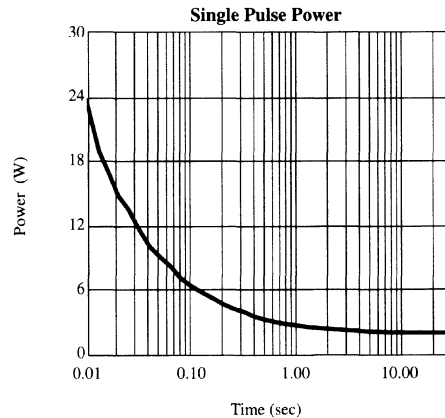
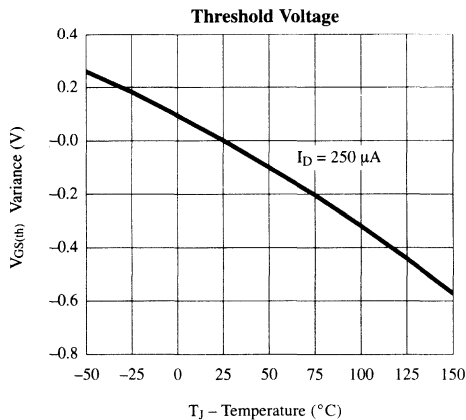
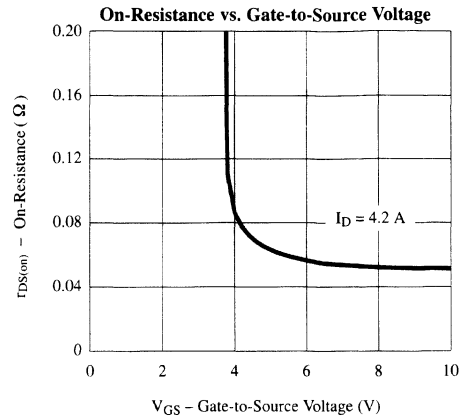
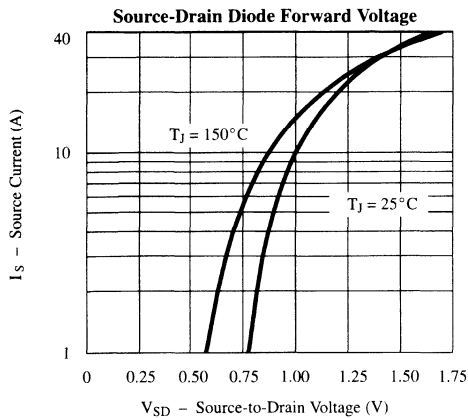
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



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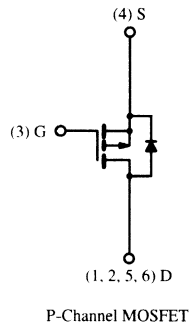
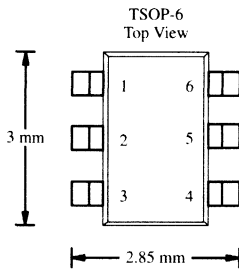
Typical Characteristics (25°C Unless Otherwise Noted)


P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.100 @ $V_{GS} = -10$ V	± 3.5
	0.190 @ $V_{GS} = -4.5$ V	± 2.5

TrenchFET™
Power MOSFETs



Power Dissipation
Si3455DV—2.0 W

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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 3.5	A
		± 2.7	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	
Maximum Power Dissipation ^a	P_D	2.0	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70194.

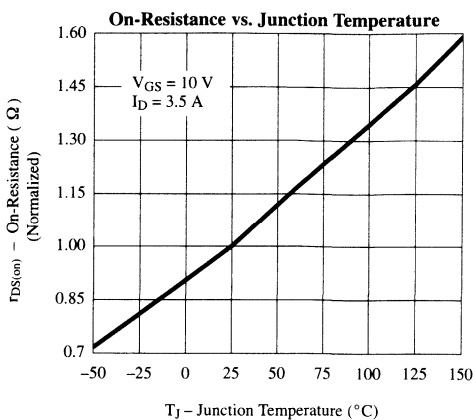
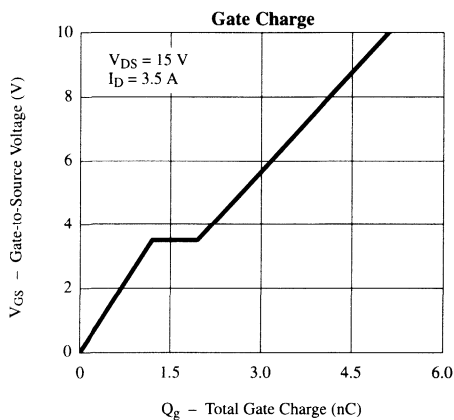
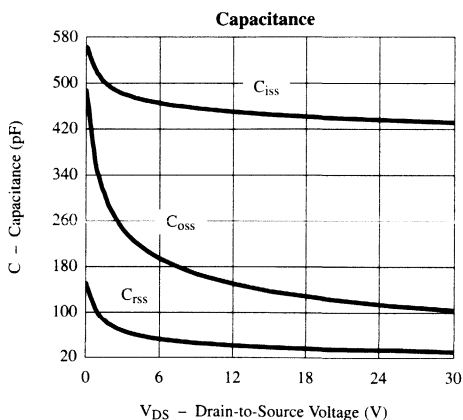
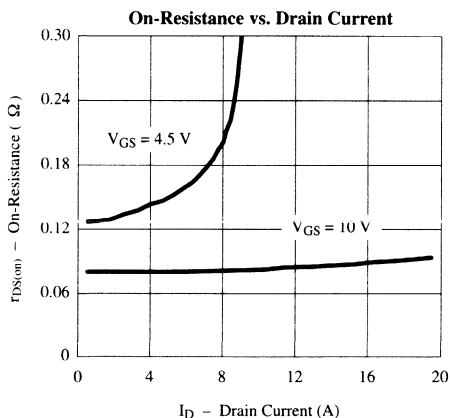
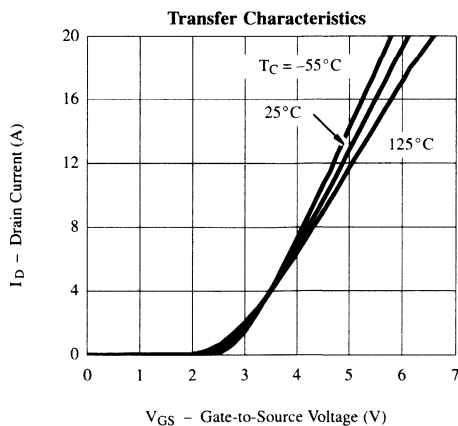
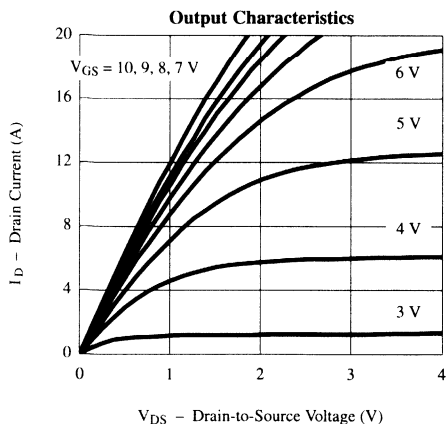
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	-15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = 3.5\ \text{A}$		0.080	0.100	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = 2.5\ \text{A}$		0.134	0.190	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -3.5\ \text{A}$		4.0		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.7\ \text{A}, V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -3.5\ \text{A}$		5.1	10	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			1.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \approx -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			20	35	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}			50	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

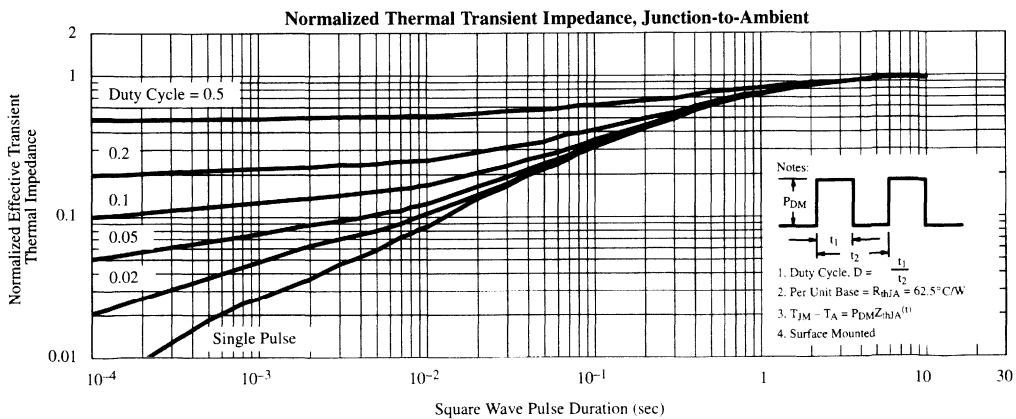
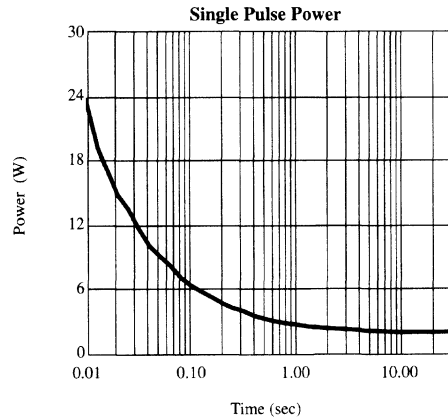
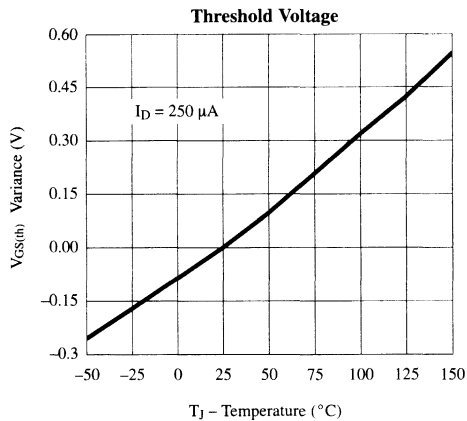
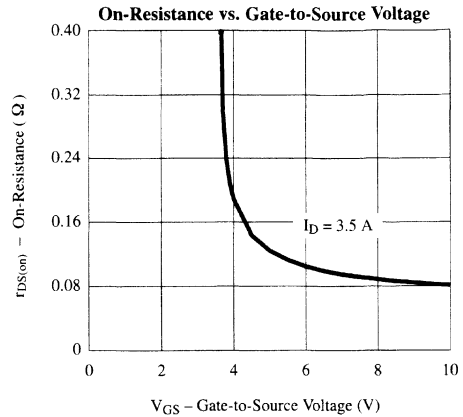
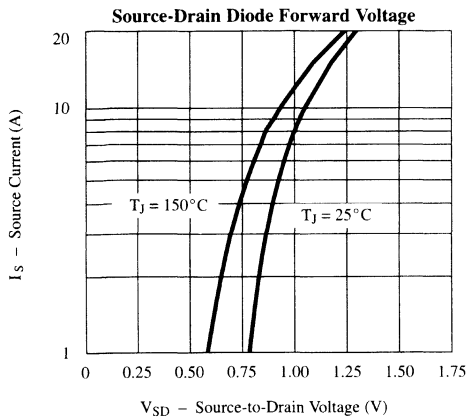
Typical Characteristics (25°C Unless Otherwise Noted)



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Typical Characteristics (25°C Unless Otherwise Noted)

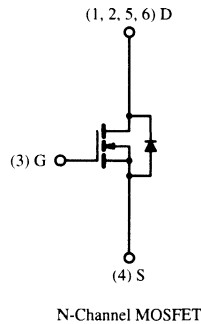
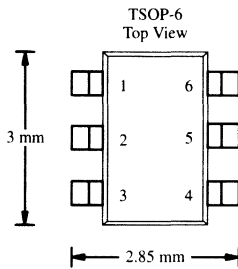


N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.045 @ $V_{GS} = 10$ V	± 5.1
	0.065 @ $V_{GS} = 4.5$ V	± 4.3

TrenchFET™
Power MOSFETs



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TSOP-6

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	± 30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 5.1	A
		± 4.1	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	± 1.7	
Maximum Power Dissipation ^a	P_D	2	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70659.

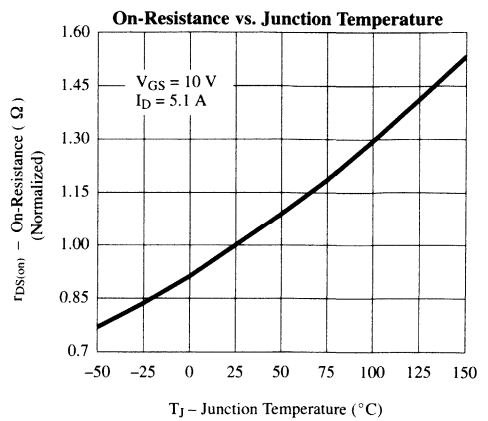
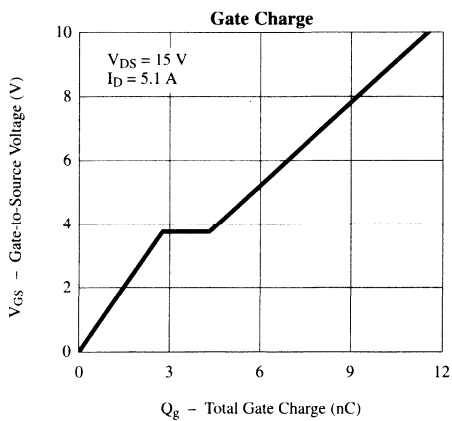
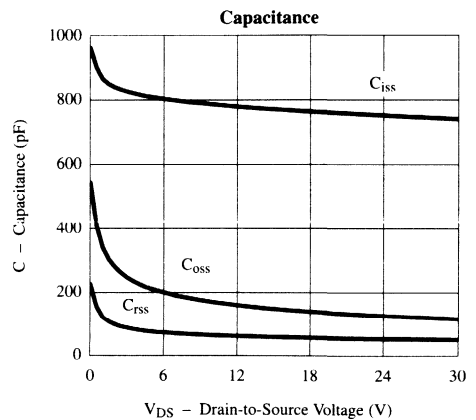
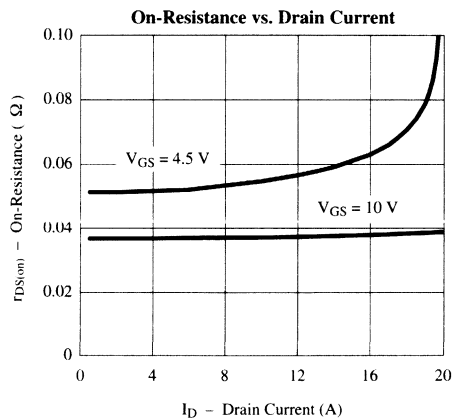
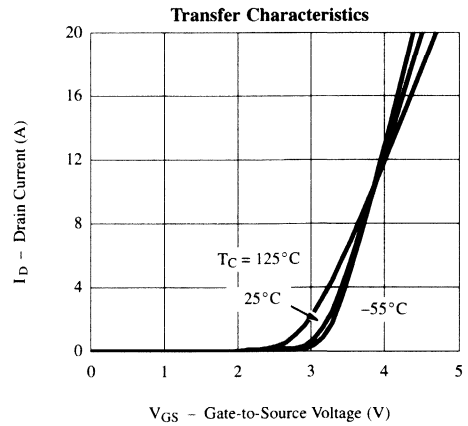
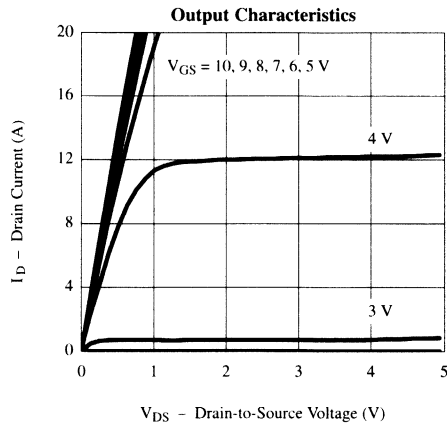
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 5.1\ \text{A}$		0.037	0.045	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 4.3\ \text{A}$		0.051	0.065	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 5.1\ \text{A}$		13		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 5.1\ \text{A}$		12	20	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	80	

Notes

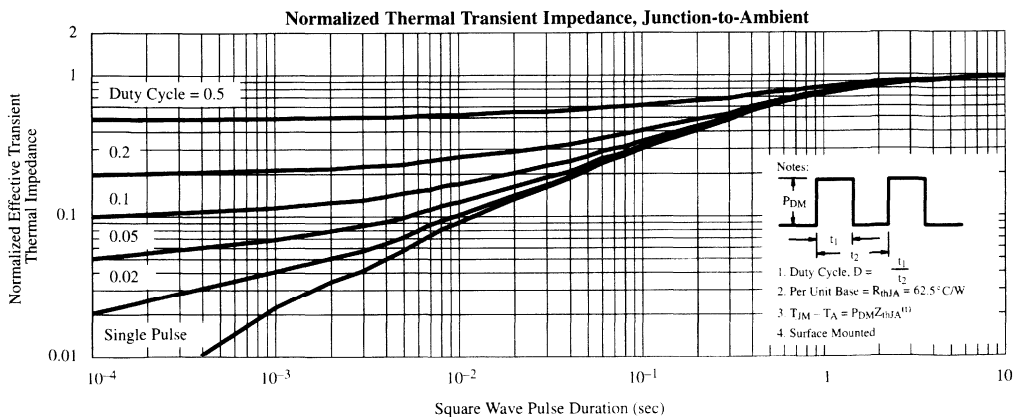
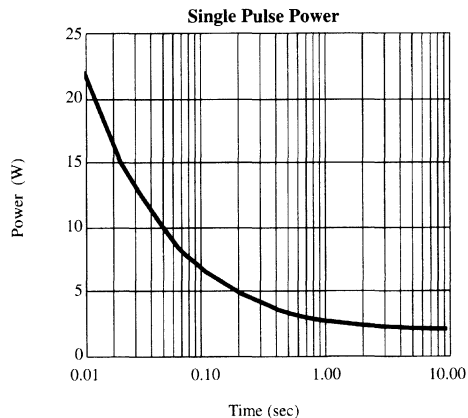
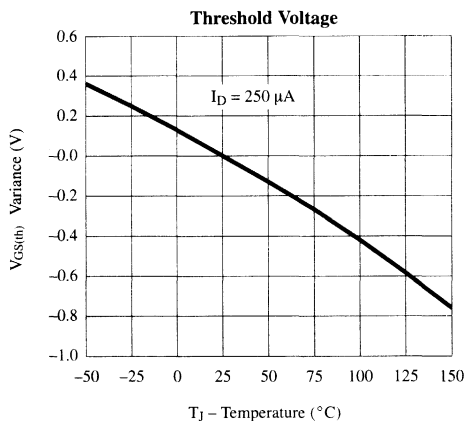
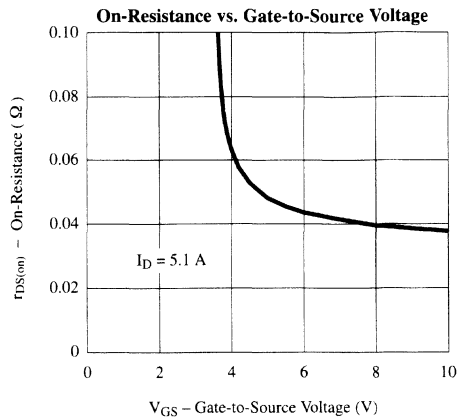
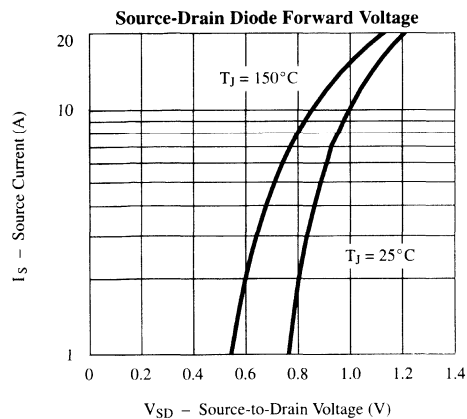
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



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TSOP-6

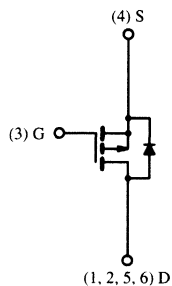
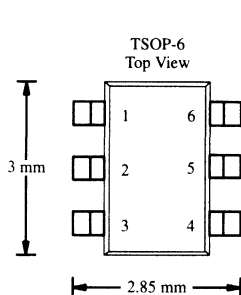
Typical Characteristics (25°C Unless Otherwise Noted)


P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.065 @ $V_{GS} = -10$ V	± 4.3
	0.100 @ $V_{GS} = -4.5$ V	± 3.4

TrenchFET™
Power MOSFETs



P-Channel MOSFET

Power Dissipation

Si3457DV—2.0 W

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TSOP-6

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 4.3	A
	$T_A = 70^\circ\text{C}$		± 3.4	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a		I_S	-1.7	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70644.

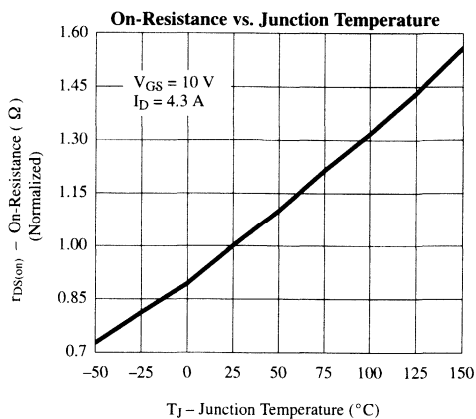
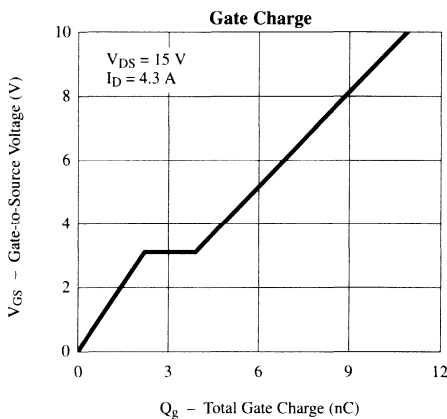
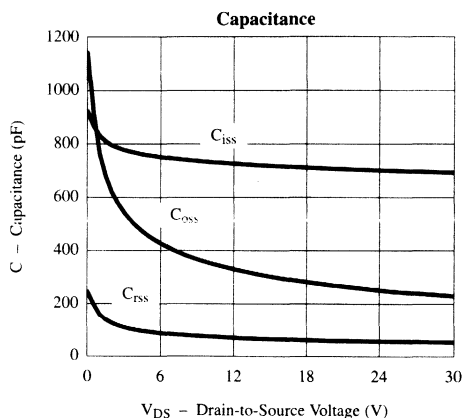
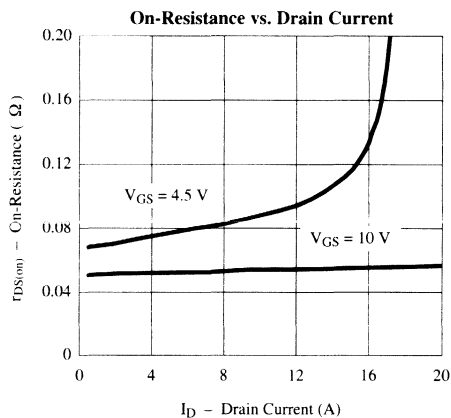
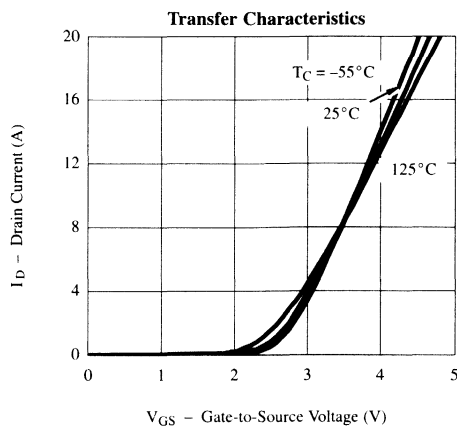
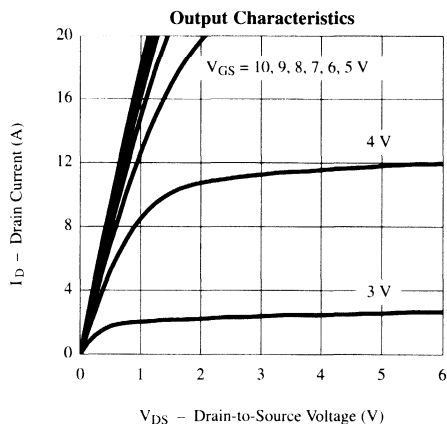
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	-15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -4.3\ \text{A}$			0.065	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -3.4\ \text{A}$			0.100	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -4.3\ \text{A}$		6		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.7\ \text{A}, V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -4.3\ \text{A}$		11	20	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			1.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}, R_L = 15\ \Omega$ $I_D \approx -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		7	15	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			30	50	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

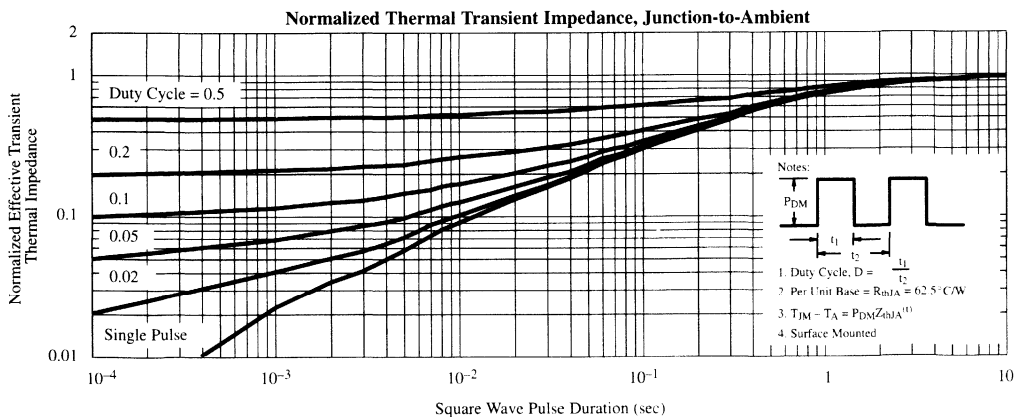
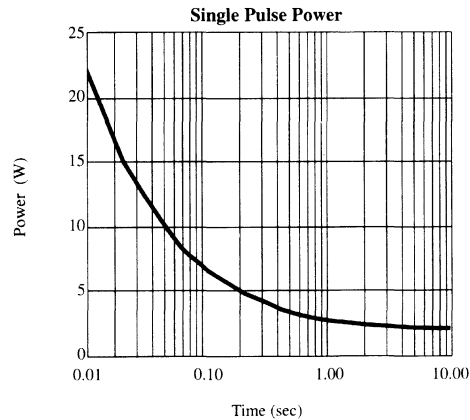
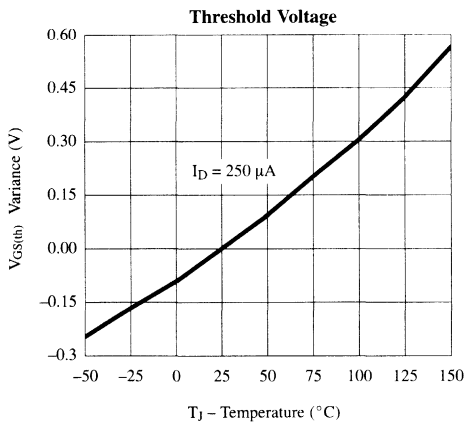
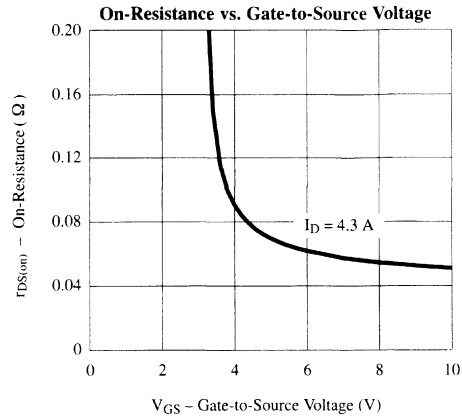
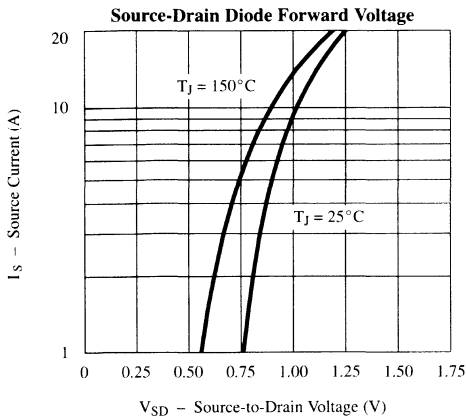
Typical Characteristics (25°C Unless Otherwise Noted)



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TSOP-6

Typical Characteristics (25°C Unless Otherwise Noted)



Selector Guides

TSSOP-8

TSSOP-8

2

SOIC-5

Application Specific Standard MOSFETs (ASSM)

Appendix

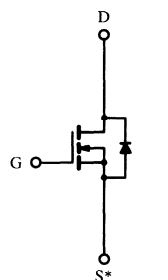
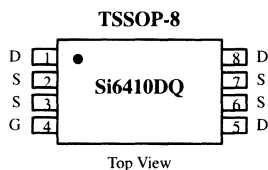
Worldwide Sales Offices and Distributors

N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.014 @ $V_{GS} = 10$ V	± 7.8
	0.021 @ $V_{GS} = 4.5$ V	± 6.3

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Power MOSFETs



*Source Pins 2, 3, 6 and 7 must be tied common.

N-Channel MOSFET

2

TSSOP-8

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 7.8	A
		± 6.2	
Pulsed Drain Current	I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I_S	1.5	W
Maximum Power Dissipation ^a	P_D	1.5	
		1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	83	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70661.

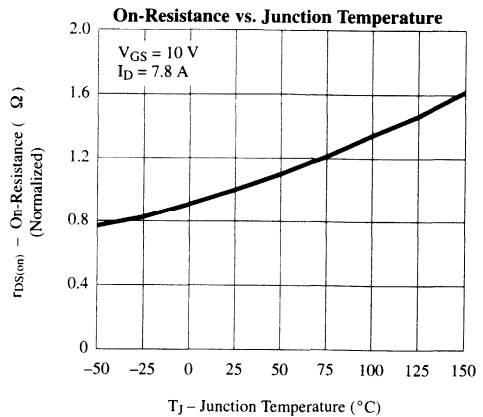
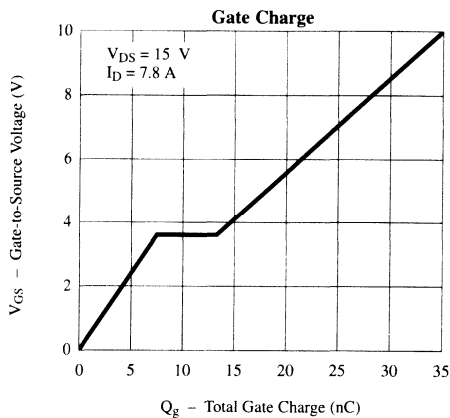
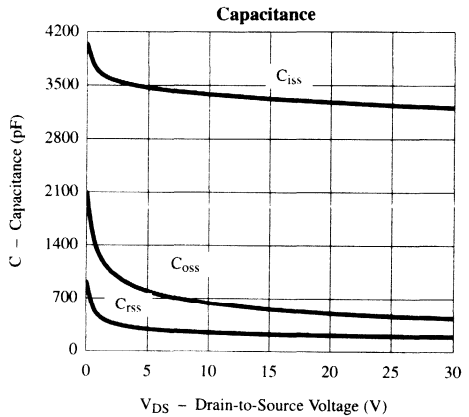
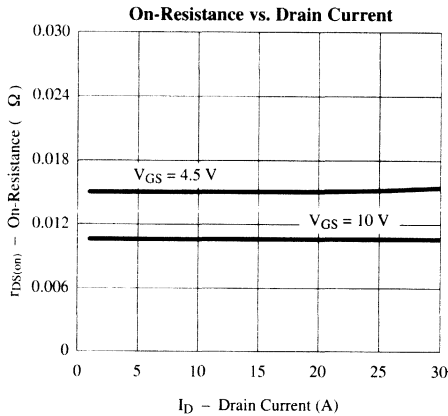
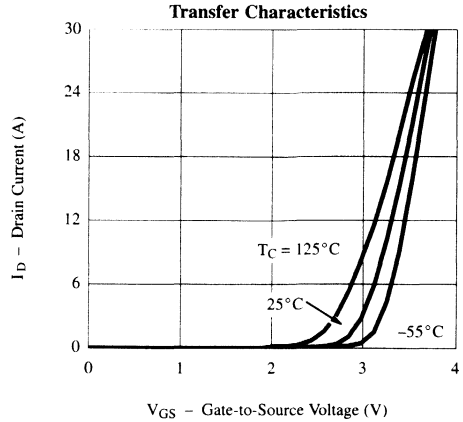
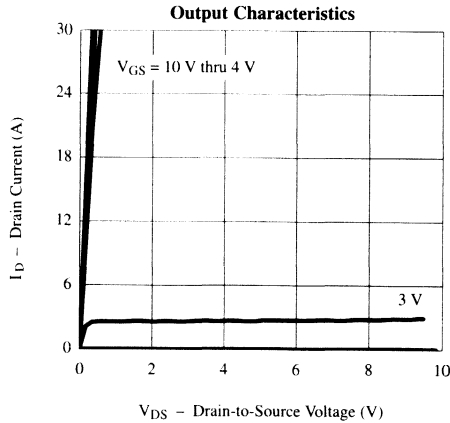
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 7.8\ \text{A}$		0.011	0.014	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 5\ \text{A}$		0.015	0.021	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 7.8\ \text{A}$		27		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.5\ \text{A}, V_{GS} = 0\ \text{V}$		0.7	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 7.8\ \text{A}$		35	60	nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			5.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		15	30	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			70	120	
Fall Time	t_f			20	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

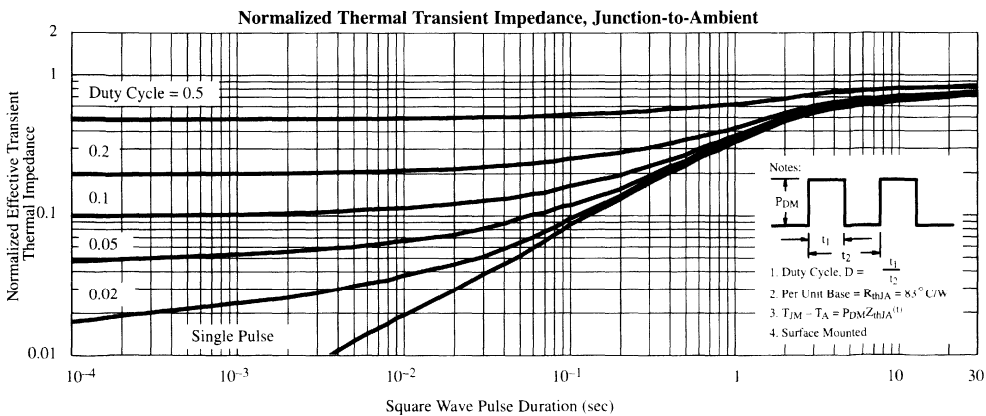
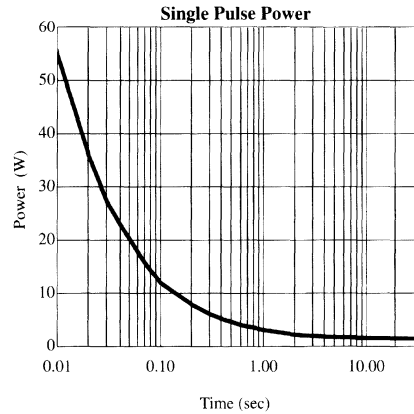
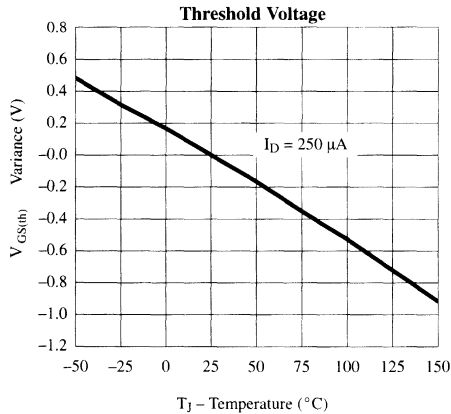
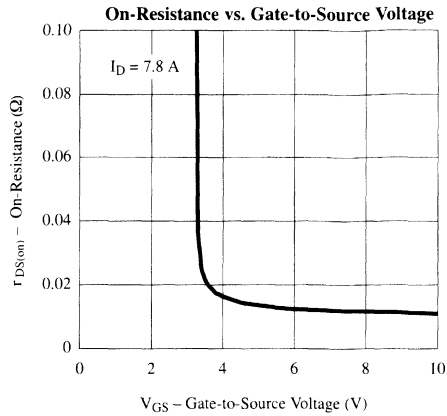
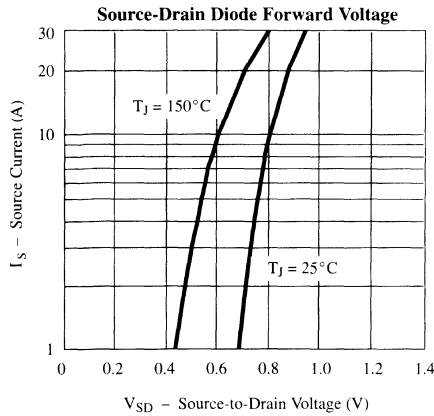
Typical Characteristics (25°C Unless Otherwise Noted)



2

TSSOP-8

Typical Characteristics (25°C Unless Otherwise Noted)

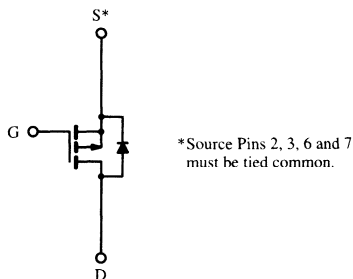
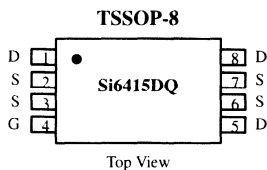


P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.019 @ $V_{GS} = -10$ V	± 6.5
	0.030 @ $V_{GS} = -4.5$ V	± 5.2

TrenchFET™
Power MOSFETS



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 6.5	A
	$T_A = 70^\circ\text{C}$		± 5.2	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a		I_S	-1.5	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.5	W
	$T_A = 70^\circ\text{C}$		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	83	°C/W

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70639.

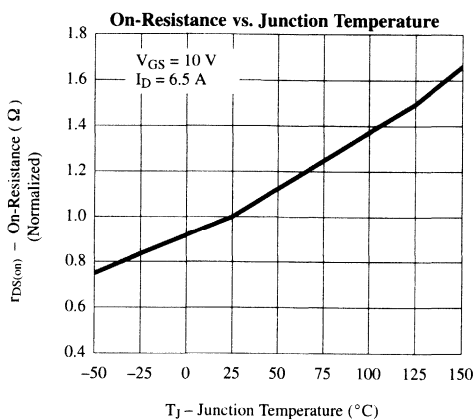
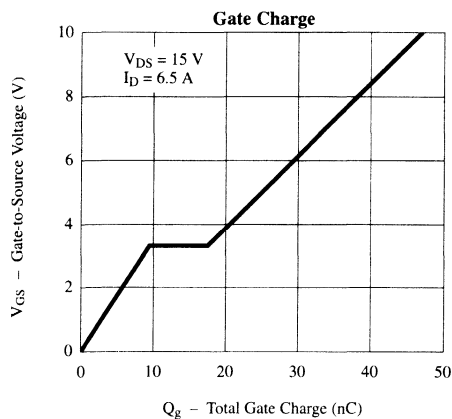
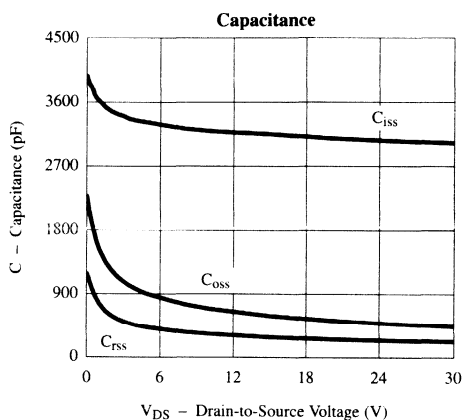
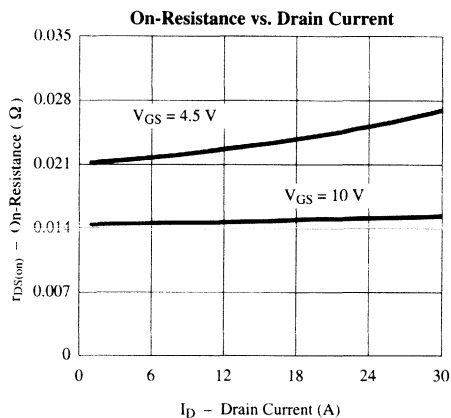
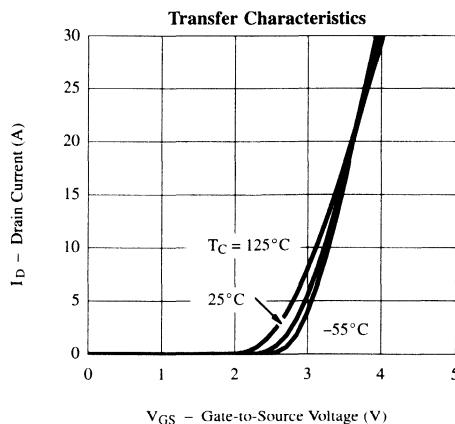
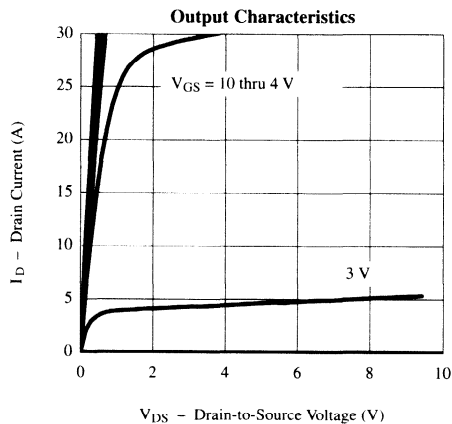
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	-20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -6.5\ \text{A}$		0.015	0.019	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -5.2\ \text{A}$		0.022	0.030	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -6.5\ \text{A}$		18.5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.5\ \text{A}, V_{GS} = 0\ \text{V}$		-0.75	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -6.5\ \text{A}$		47	70	nC
Gate-Source Charge	Q_{gs}			9.5		
Gate-Drain Charge	Q_{gd}			8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			17	30	
Turn-Off Delay Time	$t_{d(off)}$			73	110	
Fall Time	t_f			31	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		40	60	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

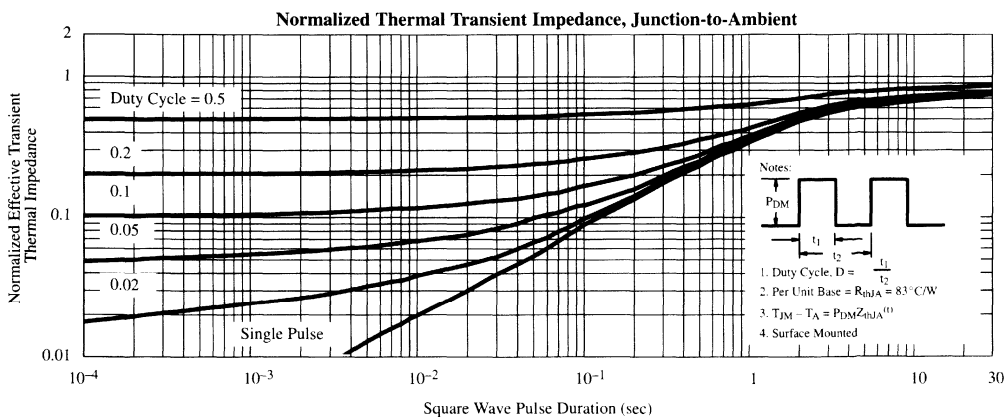
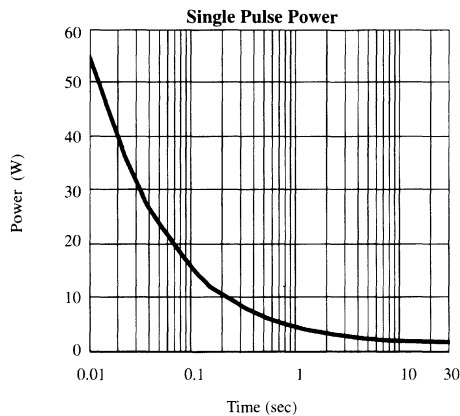
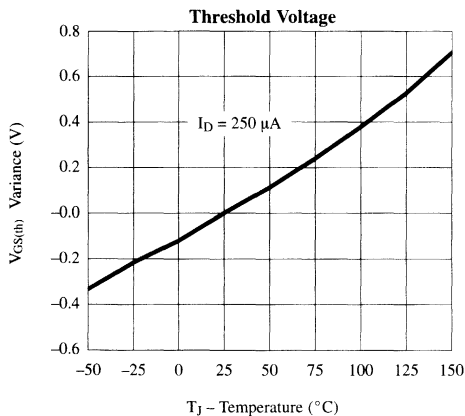
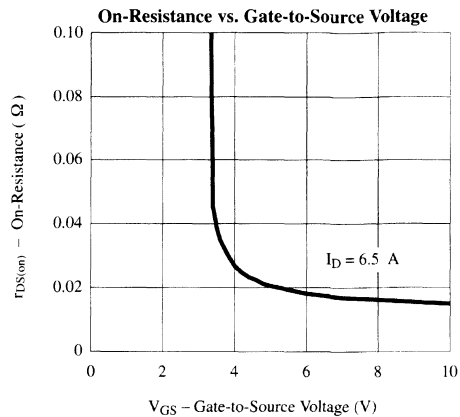
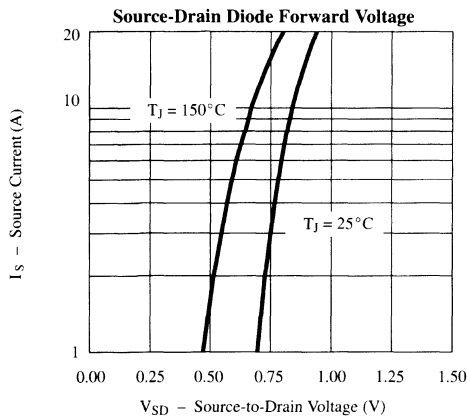
Typical Characteristics (25°C Unless Noted)



2

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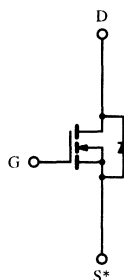
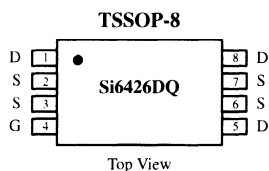
Typical Characteristics (25°C Unless Noted)



N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.035 @ $V_{GS} = 4.5$ V	± 5.4
	0.04 @ $V_{GS} = 2.5$ V	± 4.9



*Source Pins 2, 3, 6, and 7 must be tied common.

N-Channel MOSFET

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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 5.4	A
		± 4.2	
Pulsed Drain Current	I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I_S	1.25	
Maximum Power Dissipation ^a	P_D	1.5	W
		1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	83	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70174. A SPICE Model data sheet is available for this product (FaxBack document #70545).

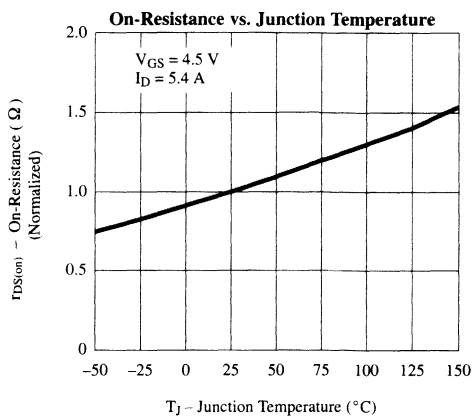
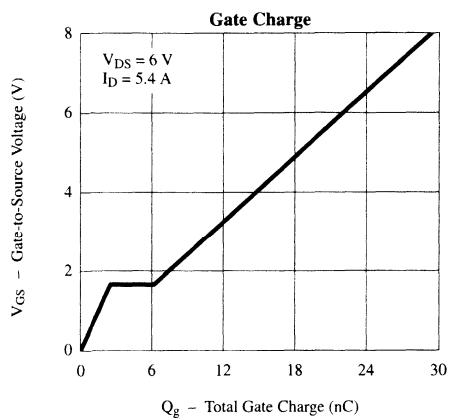
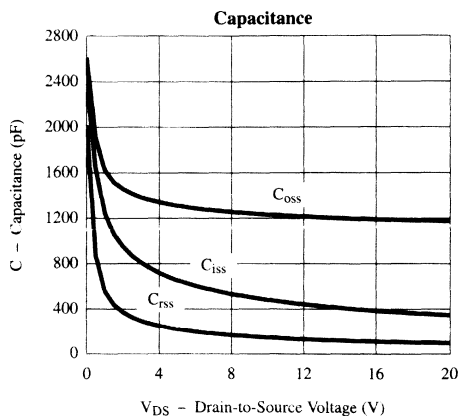
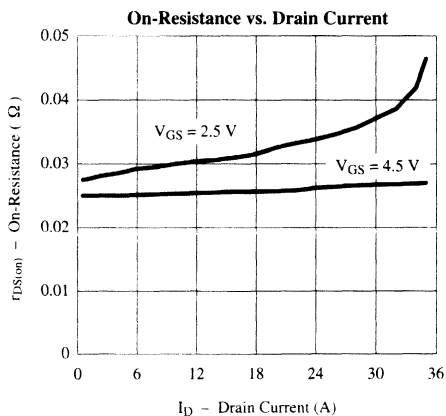
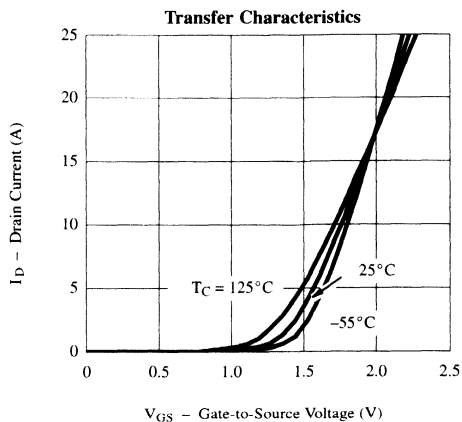
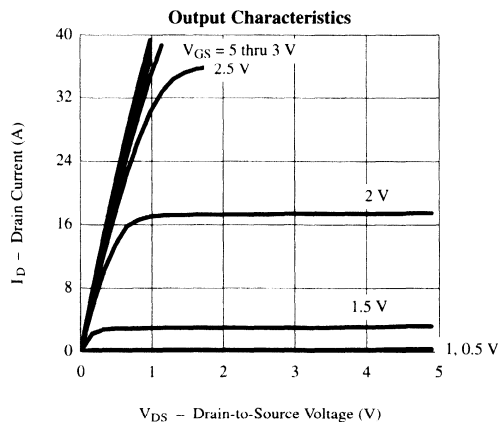
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	± 20			A
		$V_{DS} \geq 5\ \text{V}, V_{GS} = 2.5\ \text{V}$	± 8			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 5.4\ \text{A}$		0.025	0.035	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 4.9\ \text{A}$		0.030	0.04	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 5.4\ \text{A}$		22		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ \text{A}, V_{GS} = 0\ \text{V}$		0.7	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 6\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 5.4\ \text{A}$		18	35	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\ \text{V}, R_L = 6\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		35	60	ns
Rise Time	t_r			65	100	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			33	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	100	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

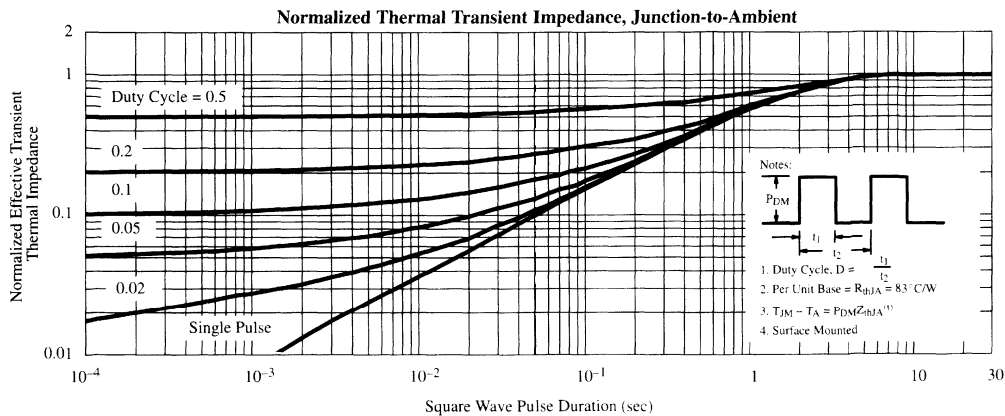
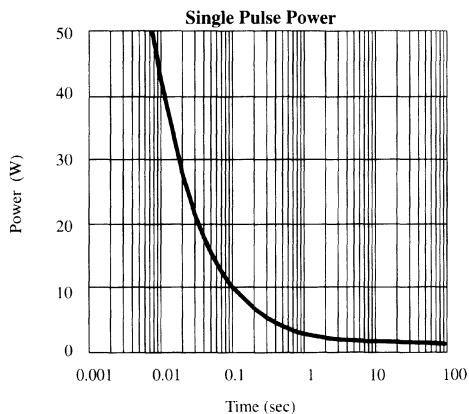
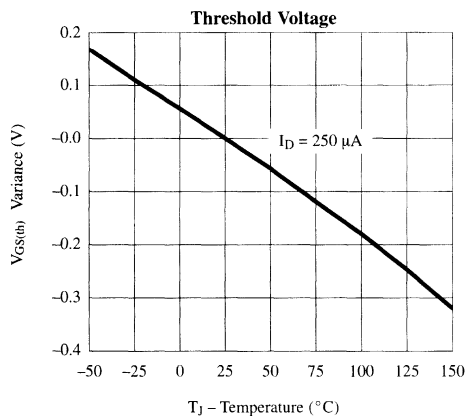
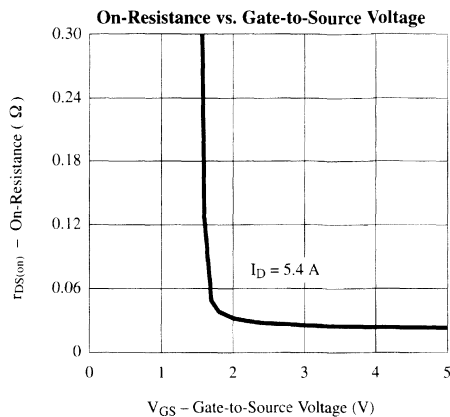
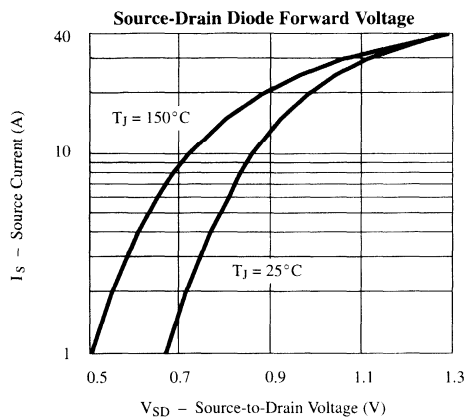
Typical Characteristics (25°C Unless Otherwise Noted)



2

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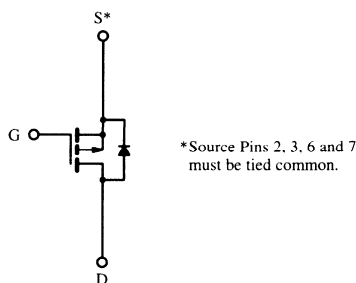
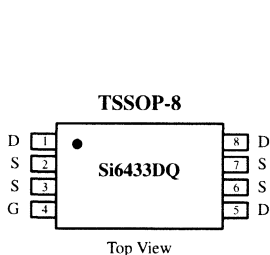
Typical Characteristics (25°C Unless Otherwise Noted)



P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-12	0.06 @ V _{GS} = -4.5 V	± 4.0
	0.09 @ V _{GS} = -2.5 V	± 3.0



P-Channel MOSFET

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TSSOP-8

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-12	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 4.0	A
		± 3.2	
Pulsed Drain Current	I _{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I _S	-1.4	
Maximum Power Dissipation ^a	P _D	1.5	W
		1.0	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	83	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70168. A SPICE Model data sheet is available for this product (FaxBack document #70530).

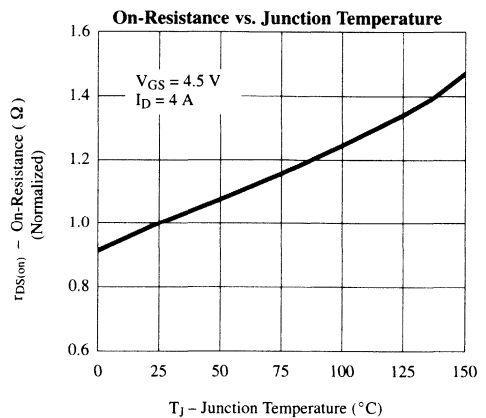
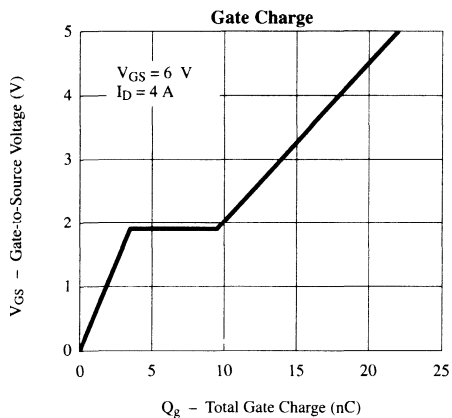
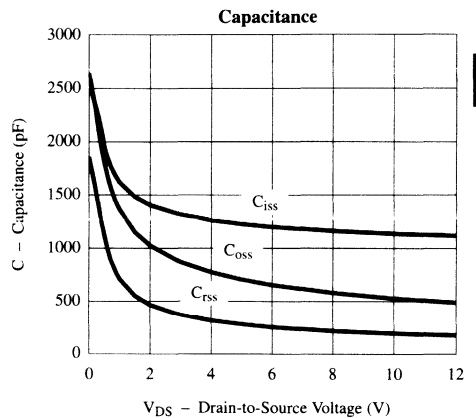
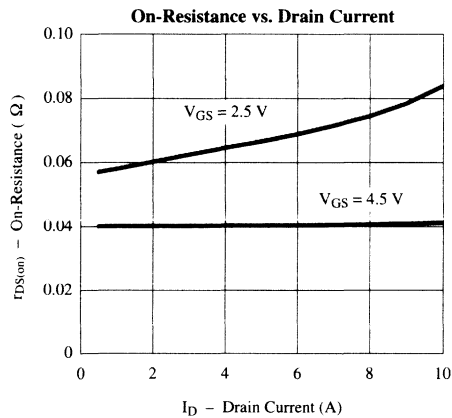
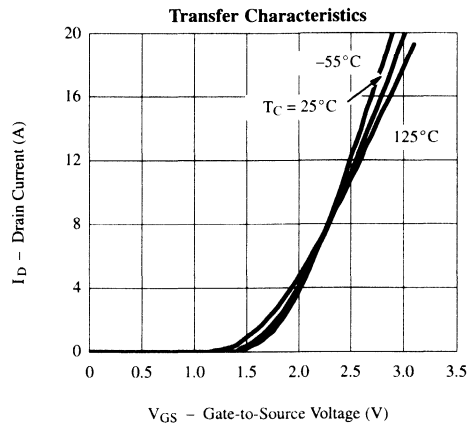
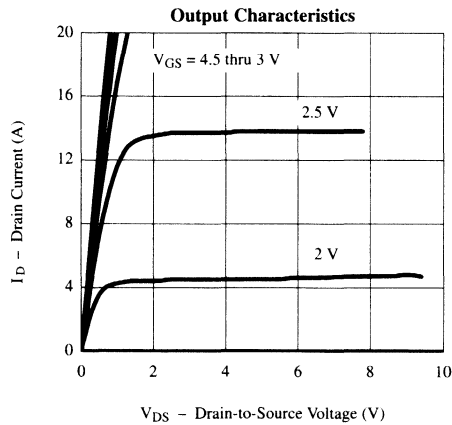
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -12\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-10			A
		$V_{DS} = -5\ \text{V}, V_{GS} = -2.5\ \text{V}$	-4			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = 4.0\ \text{A}$		0.040	0.06	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = 2.0\ \text{A}$		0.060	0.09	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -9\ \text{V}, I_D = -4.0\ \text{A}$		13		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.4\ \text{A}, V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -4.0\ \text{A}$		20	40	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			6.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\ \text{V}, R_L = 6\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		26	60	ns
Rise Time	t_r			47	100	
Turn-Off Delay Time	$t_{d(off)}$			87	180	
Fall Time	t_f			47	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.4\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		70	100	

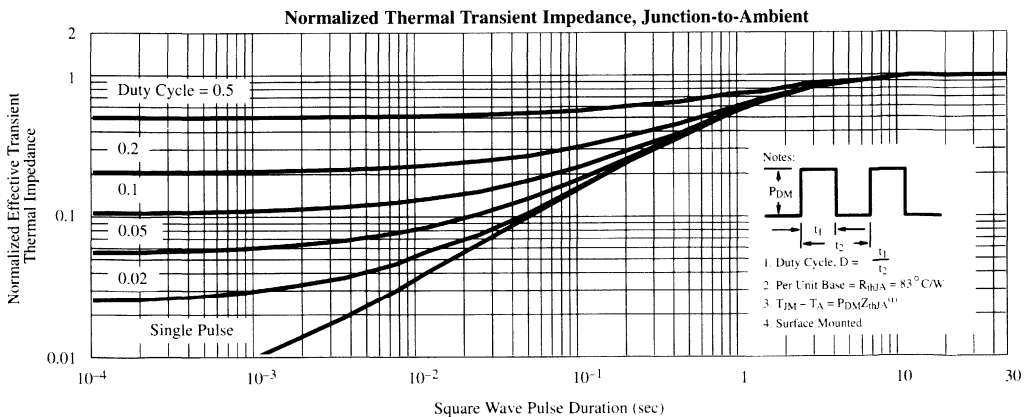
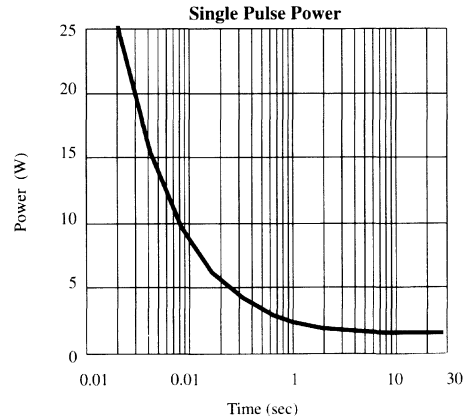
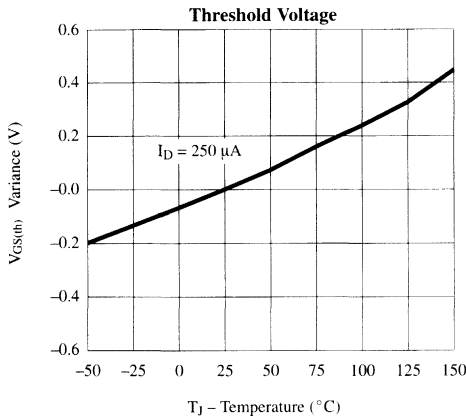
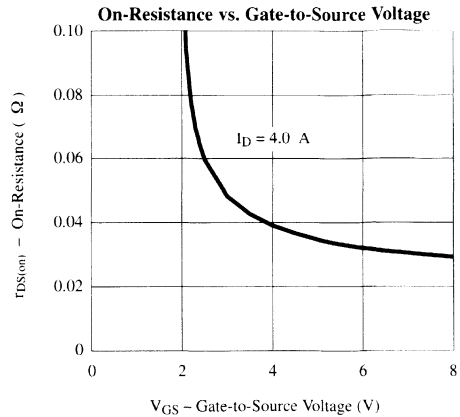
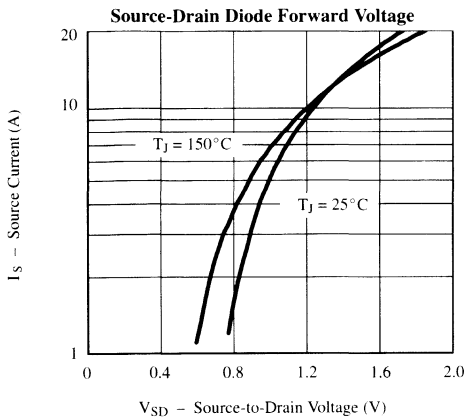
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



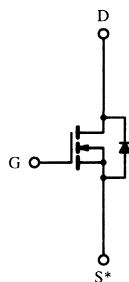
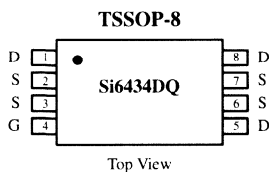
Typical Characteristics (25°C Unless Noted)



N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
30	0.028 @ V _{GS} = 10 V	± 5.6
	0.042 @ V _{GS} = 4.5 V	± 4.5



*Source Pins 2, 3, 6 and 7 must be tied common.

N-Channel MOSFET

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TSSOP-8

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 5.6	A
		± 4.4	
Pulsed Drain Current	I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I _S	1.25	
Maximum Power Dissipation ^a	P _D	1.5	W
		1.0	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	83	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70178. A SPICE Model data sheet is available for this product (FaxBack document #70562).

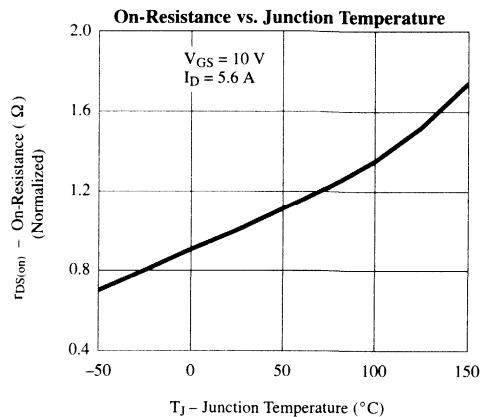
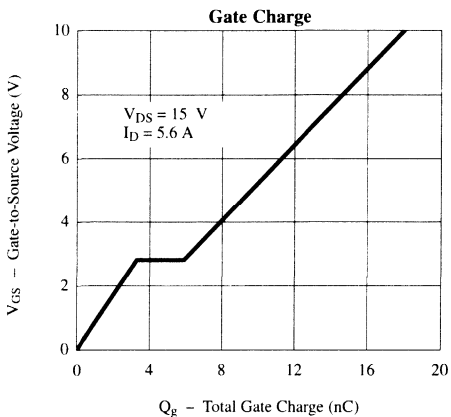
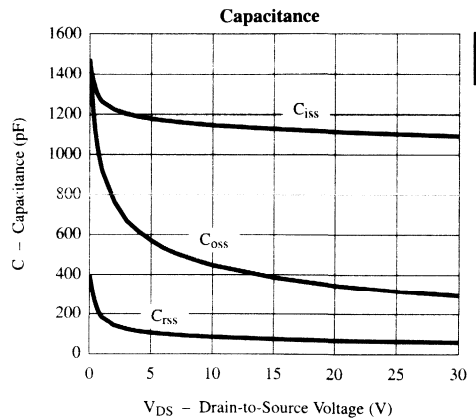
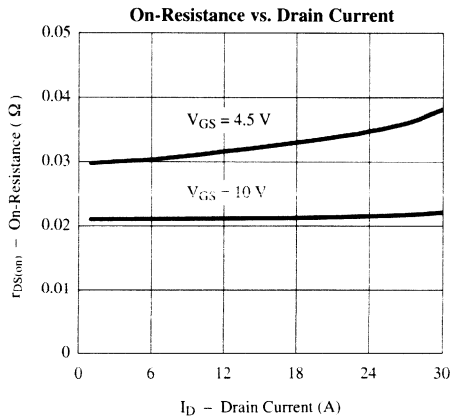
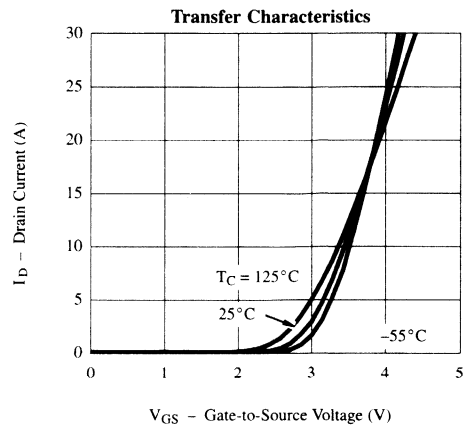
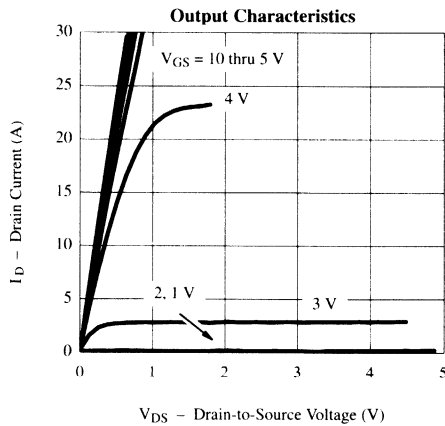
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 5.6\ \text{A}$		0.022	0.028	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 3.5\ \text{A}$		0.030	0.042	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 5.6\ \text{A}$		14		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ \text{A}, V_{GS} = 0\ \text{V}$		0.75	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 5.6\ \text{A}$		18	29	nC
Gate-Source Charge	Q_{gs}			3.3		
Gate-Drain Charge	Q_{gd}			2.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D = 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		9	15	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			38	55	
Fall Time	t_f			19	28	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		45		

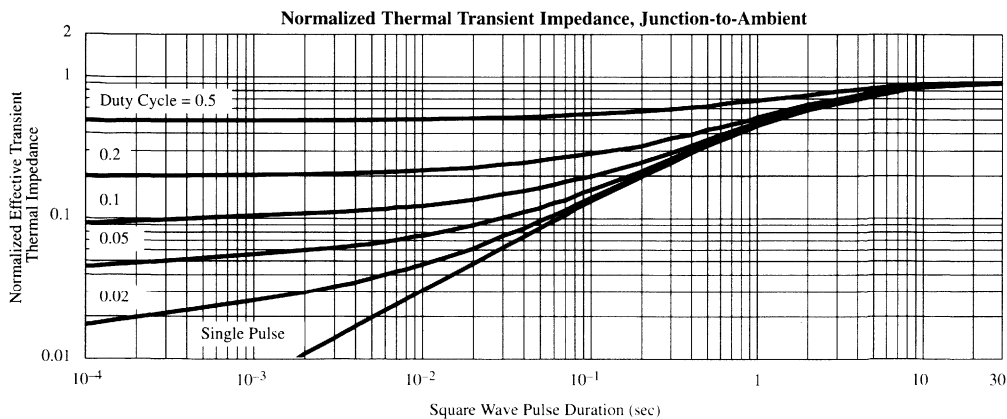
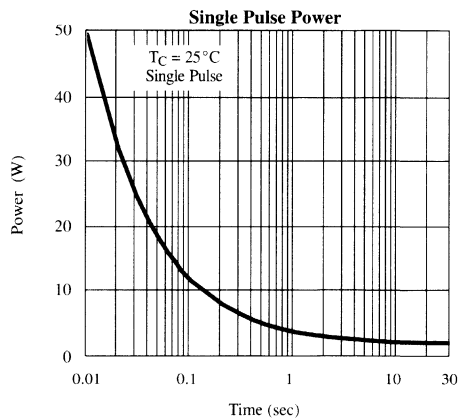
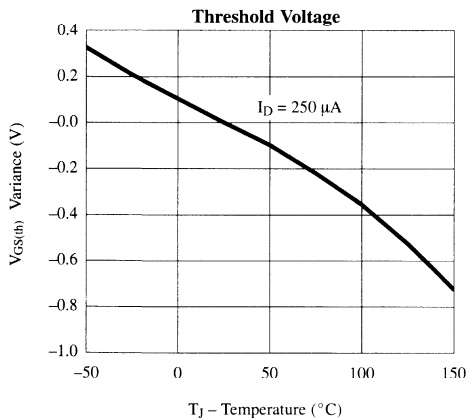
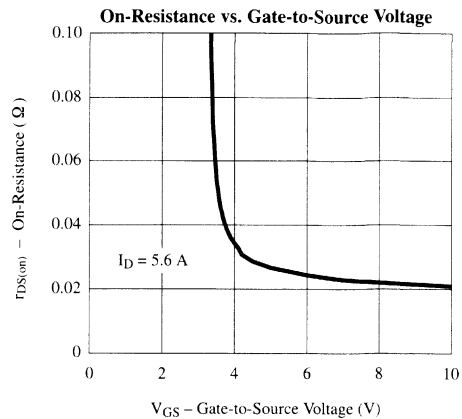
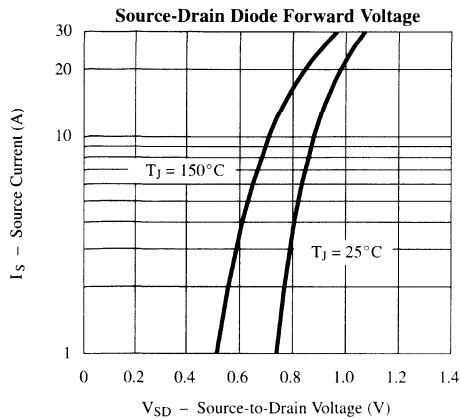
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)



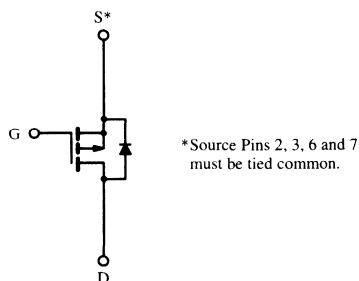
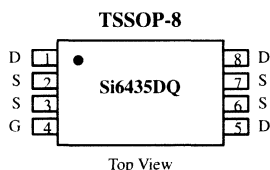
Typical Characteristics (25°C Unless Otherwise Noted)



P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-30	0.040 @ V _{GS} = -10 V	± 4.5
	0.070 @ V _{GS} = -4.5 V	± 3.4



P-Channel MOSFET

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Absolute Maximum Ratings (T_A = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C) ^a	I _D	± 4.5	A
		± 3.6	
Pulsed Drain Current	I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I _S	-1.25	
Maximum Power Dissipation ^a	P _D	1.5	W
		1.0	
Operating Junction and Storage Temperature Range	T _J , T _{sig}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	83	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70182. A SPICE Model data sheet is available for this product (FaxBack document #70546).

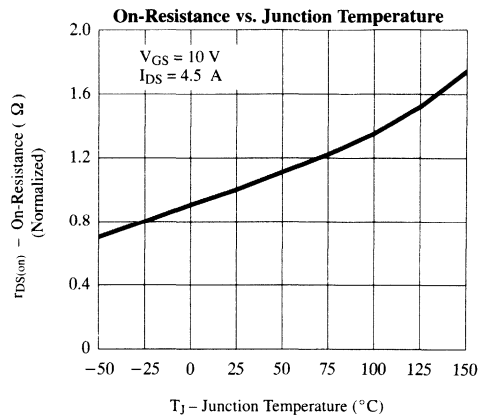
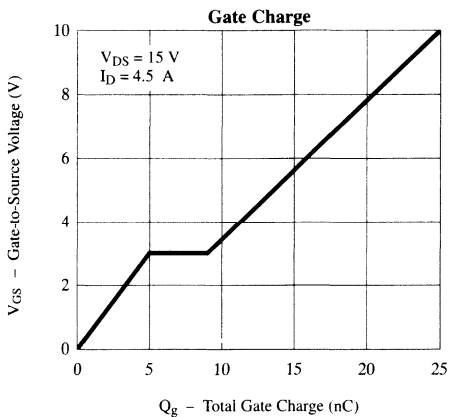
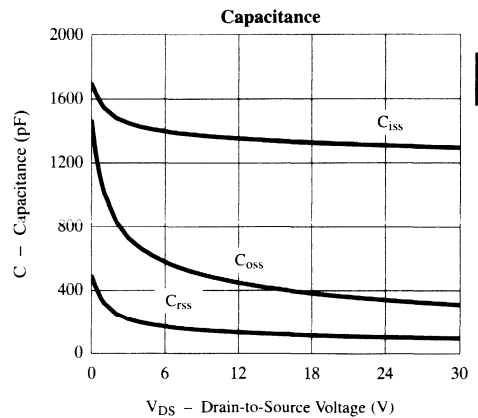
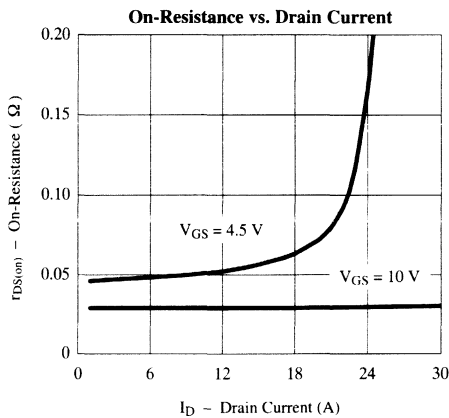
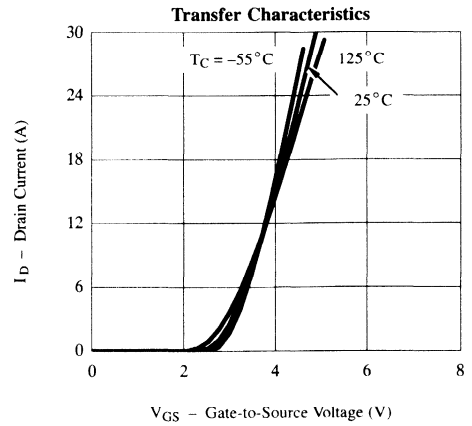
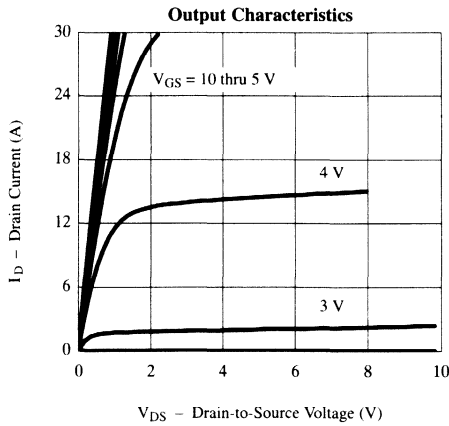
Specifications (T_J = 25° C Unless Otherwise Noted)

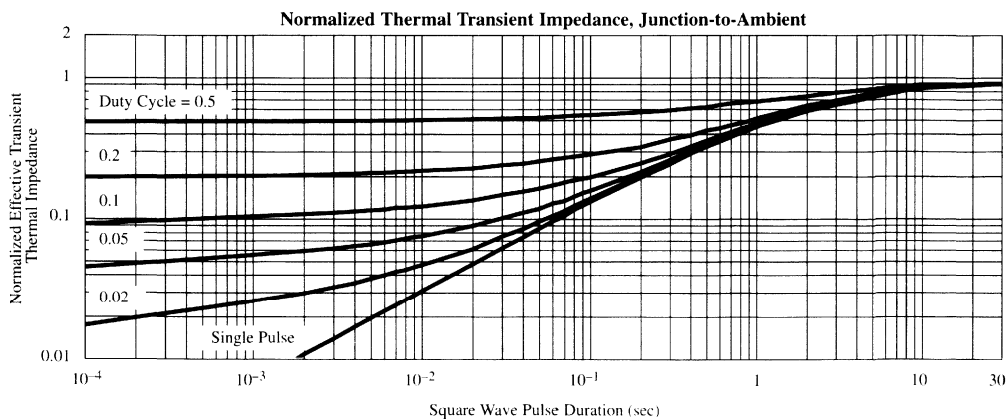
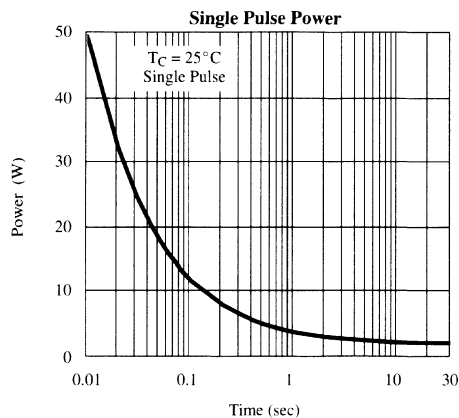
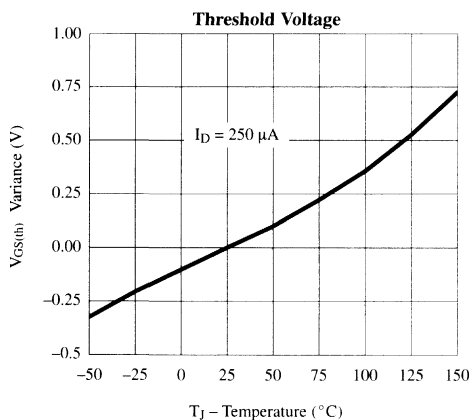
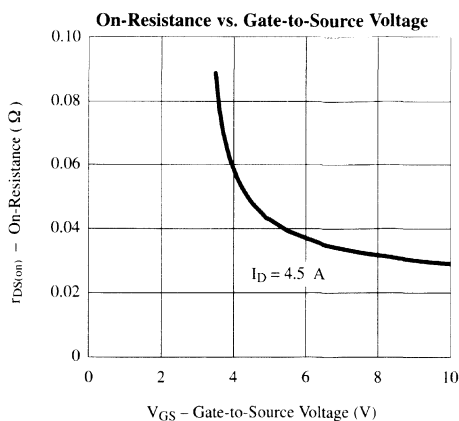
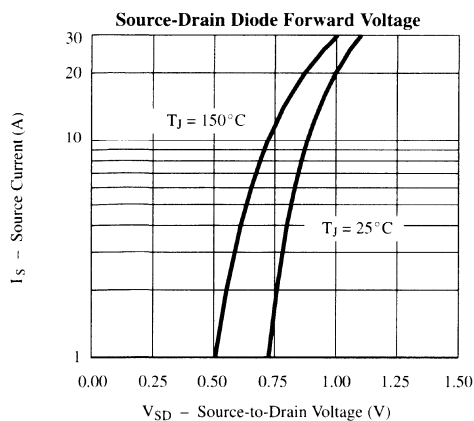
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 70°C			-25	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-30			A
		V _{DS} = -5 V, V _{GS} = -4.5 V	-7			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -4.5 A		0.029	0.040	Ω
		V _{GS} = -4.5 V, I _D = -3.4 A		0.047	0.070	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -4.5 A		9.3		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.25 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -4.5 A		25	35	nC
Gate-Source Charge	Q _{gs}			5.0		
Gate-Drain Charge	Q _{gd}			4.0		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		12	20	ns
Rise Time	t _r			13	20	
Turn-Off Delay Time	t _{d(off)}			40	55	
Fall Time	t _f			16	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.25 A, di/dt = 100 A/μs		50	80	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)



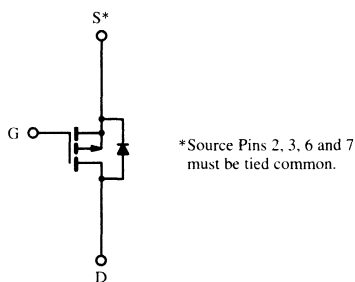
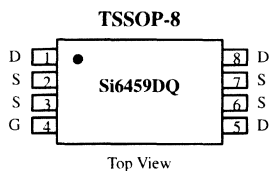
Typical Characteristics (25°C Unless Noted)


P-Channel 60-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-60	0.120 @ $V_{GS} = -10$ V	± 2.6
	0.150 @ $V_{GS} = -4.5$ V	± 2.4

TrenchFET™
Power MOSFETs



P-Channel MOSFET

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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 2.6	A
		± 2.1	
Pulsed Drain Current	I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.25	
Maximum Power Dissipation ^a	P_D	1.5	W
		1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	83	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70186.

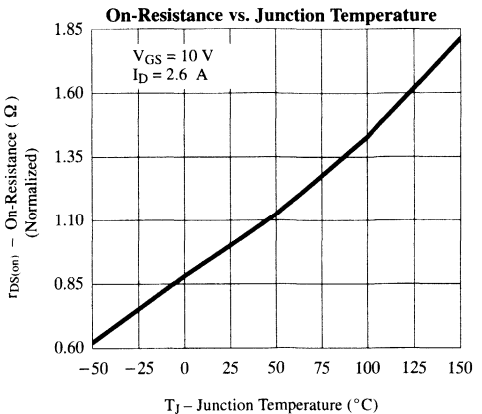
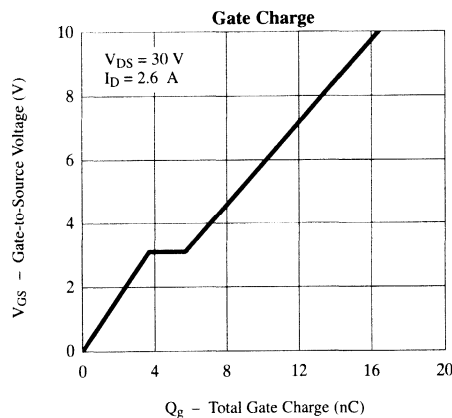
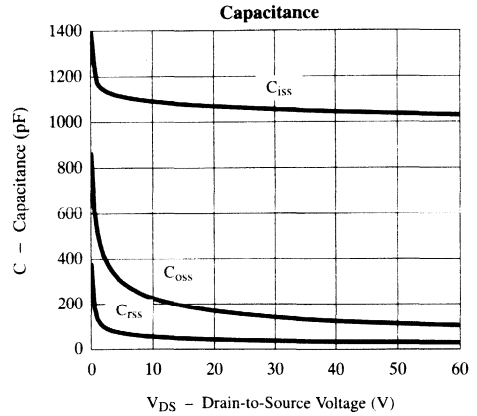
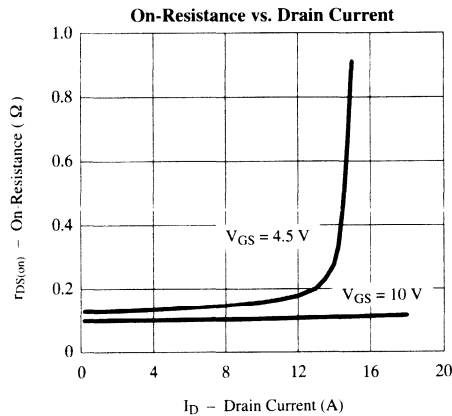
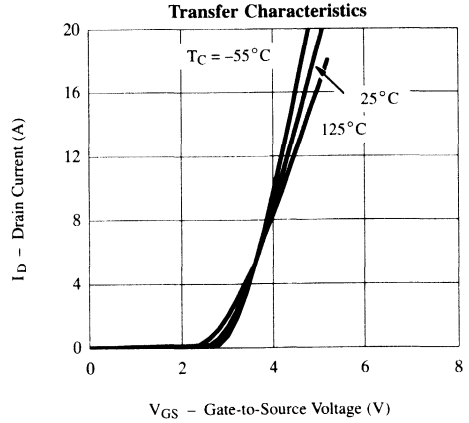
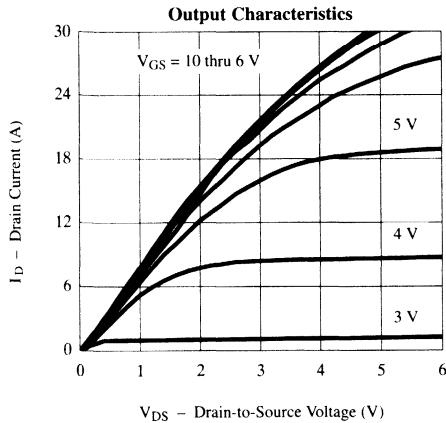
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -60\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	-20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -2.6\ \text{A}$		0.100	0.120	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -2.4\ \text{A}$		0.125	0.150	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -2.6\ \text{A}$		7.5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.25\ \text{A}, V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -30\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -2.6\ \text{A}$		16	25	nC
Gate-Source Charge	Q_{gs}			3.7		
Gate-Drain Charge	Q_{gd}			2.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\ \text{V}, R_L = 30\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		8	15	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			12	25	
Fall Time	t_f			35	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	90	

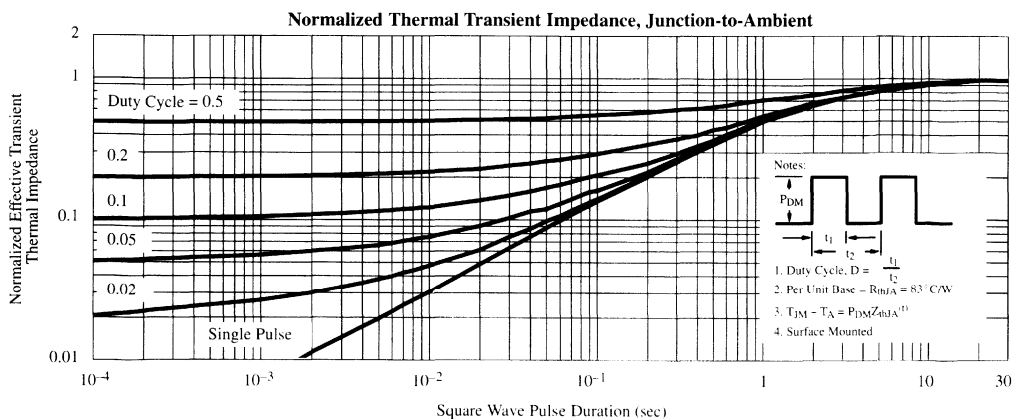
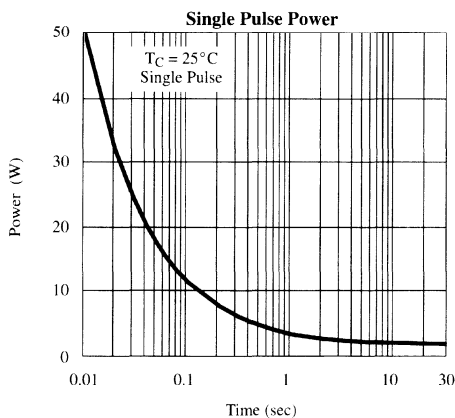
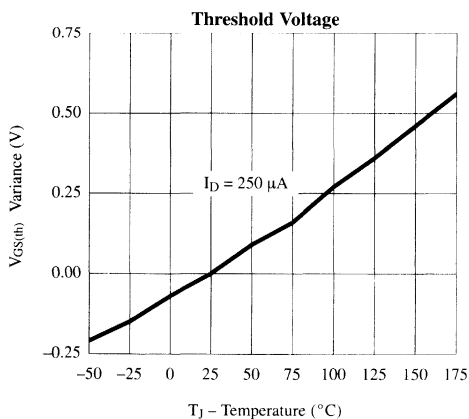
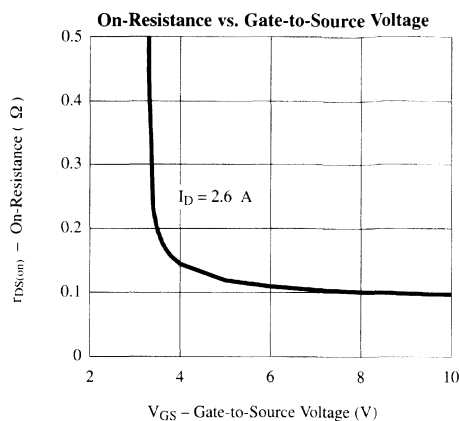
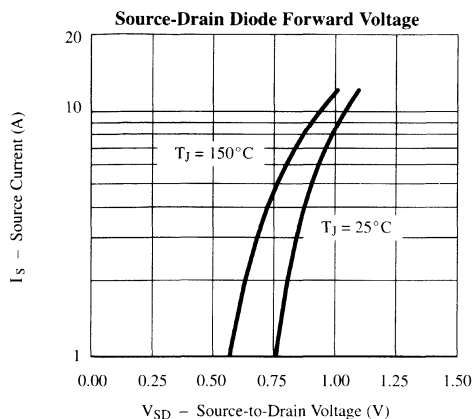
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)



Typical Characteristics (25°C Unless Noted)

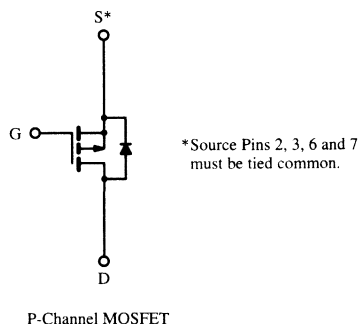
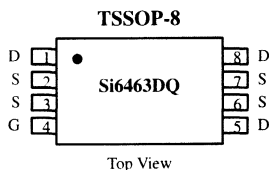


P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.020 @ $V_{GS} = -4.5$ V	± 6.5
	0.030 @ $V_{GS} = -2.5$ V	± 5.2

TrenchFET™
Power MOSFETs
2.5-V Rated



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TSSOP-8

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	−20	V
Gate-Source Voltage		V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	± 6.5	A
	T _A = 70 °C		± 5.2	
Pulsed Drain Current		I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a		I _S	−1.5	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	1.5	W
	T _A = 70 °C		1.0	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^d	R _{thJA}	83	°C/W

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70660.

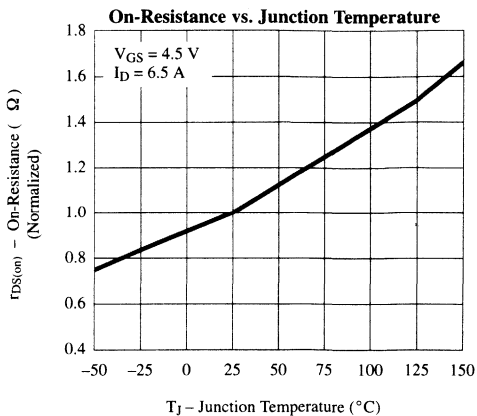
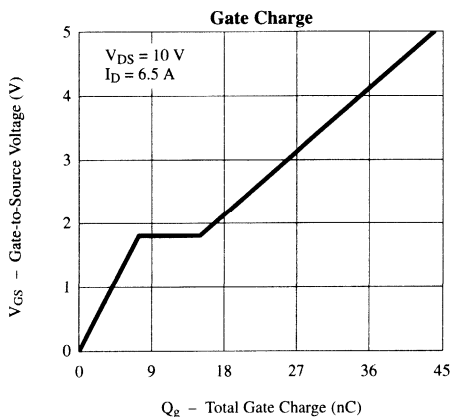
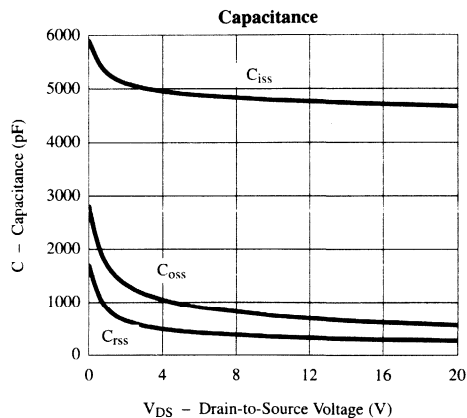
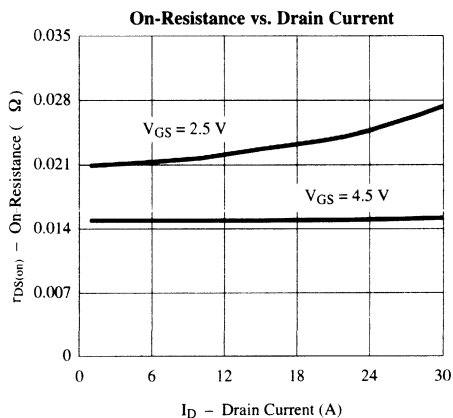
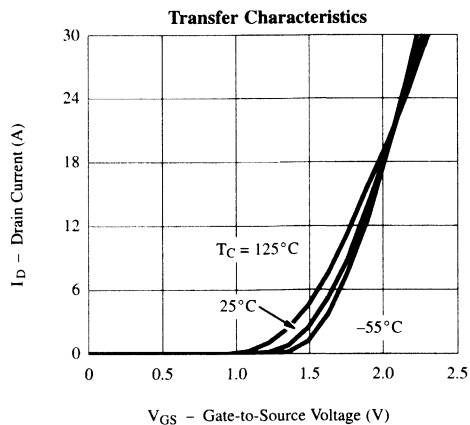
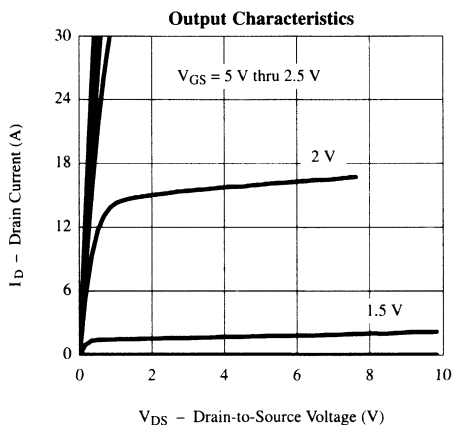
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	-20			A
		$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-10			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -6.5\ \text{A}$		0.015	0.020	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -5.2\ \text{A}$		0.022	0.030	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -6.5\ \text{A}$		26		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.5\ \text{A}, V_{GS} = 0\ \text{V}$		0.65	-1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -6.5\ \text{A}$		33	60	nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			7.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		24	50	ns
Rise Time	t_r			26	50	
Turn-Off Delay Time	$t_{d(off)}$			120	200	
Fall Time	t_f			65	110	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		40	60	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

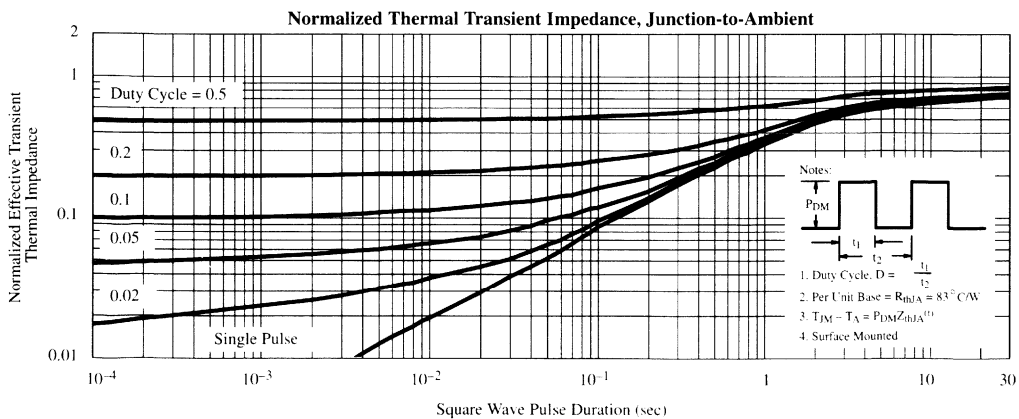
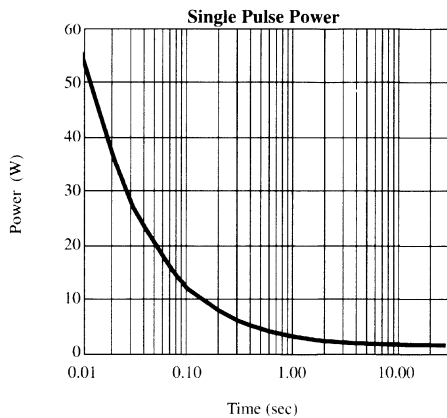
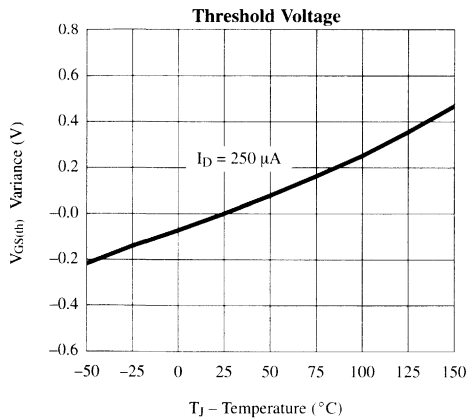
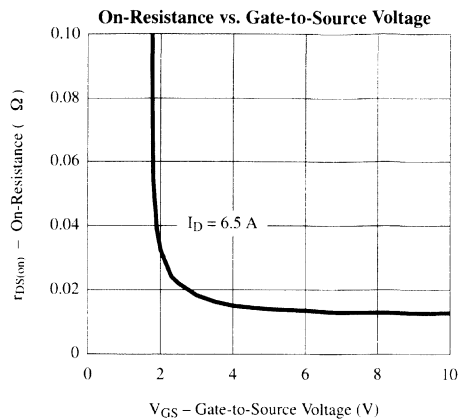
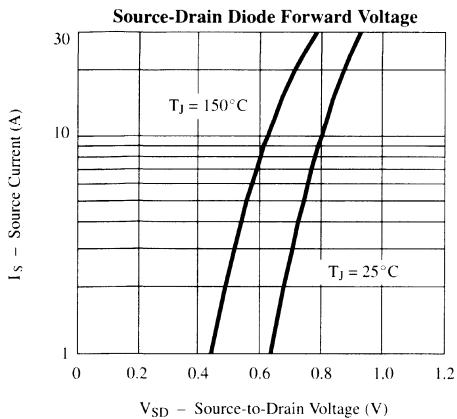
Typical Characteristics (25°C Unless Otherwise Noted)



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Typical Characteristics (25°C Unless Otherwise Noted)

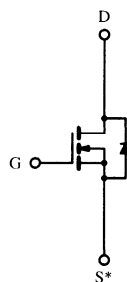
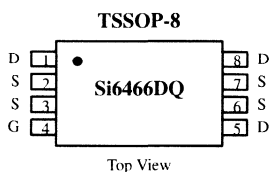


N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.014 @ V _{GS} = 4.5 V	± 7.8
	0.021 @ V _{GS} = 2.5 V	± 6.3

TrenchFET™
Power MOSFETs
2.5-V Rated



*Source Pins 2, 3, 6 and 7 must be tied common.

N-Channel MOSFET

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TSSOP-8

Absolute Maximum Ratings (T_A = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C) ^a	I _D	± 7.8	A
		± 6.2	
Pulsed Drain Current	I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I _S	1.50	
Maximum Power Dissipation ^a	P _D	1.5	W
		1.0	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	83	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70719.

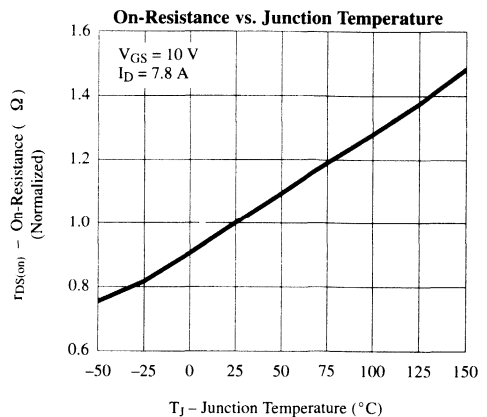
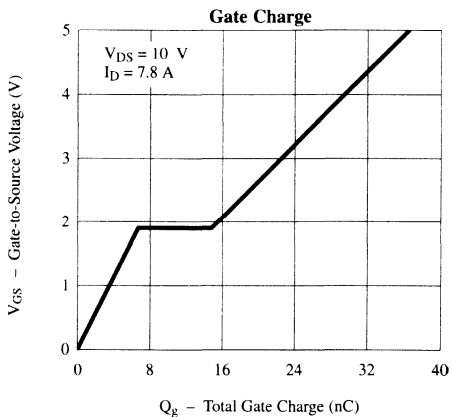
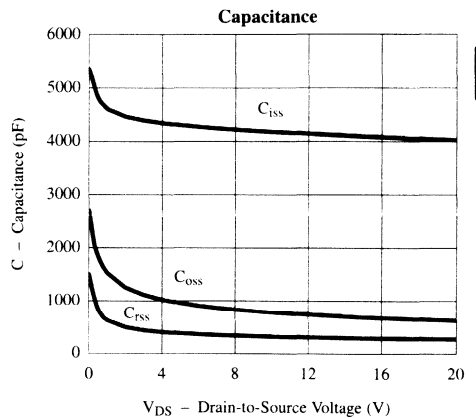
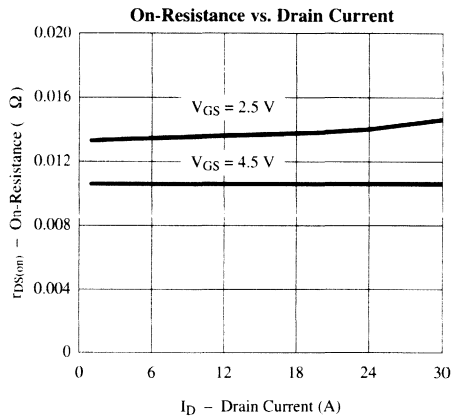
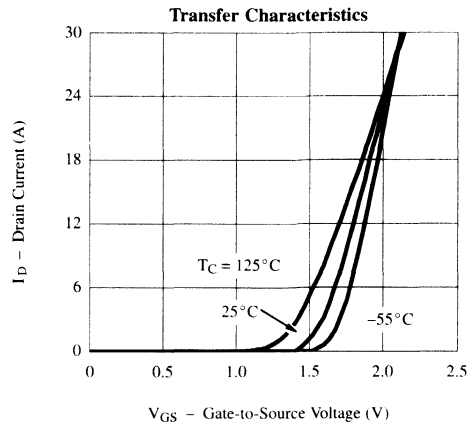
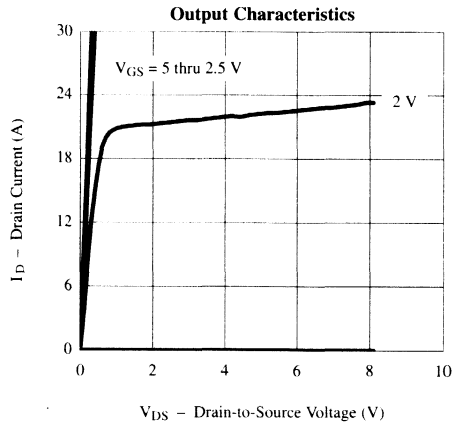
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 7.8\ \text{A}$		0.0105	0.014	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 6.3\ \text{A}$		0.0135	0.021	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 7.8\ \text{A}$		45		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.50\ \text{A}, V_{GS} = 0\ \text{V}$		0.7	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 7.8\ \text{A}$		34	60	nC
Gate-Source Charge	Q_{gs}			6.7		
Gate-Drain Charge	Q_{gd}			8.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		19	40	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			130	250	
Fall Time	t_f			40	80	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.50\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

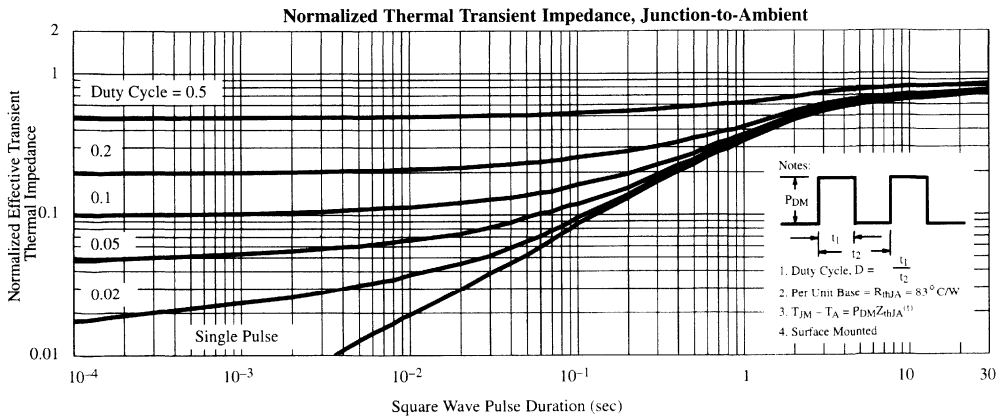
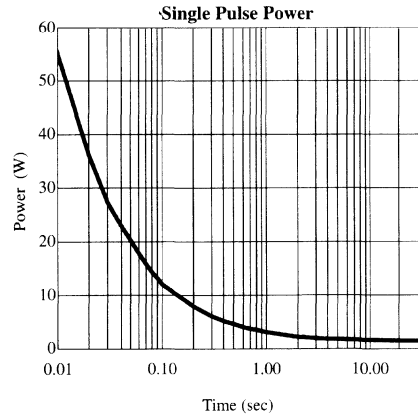
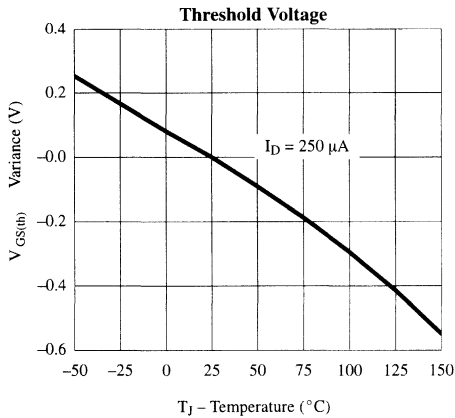
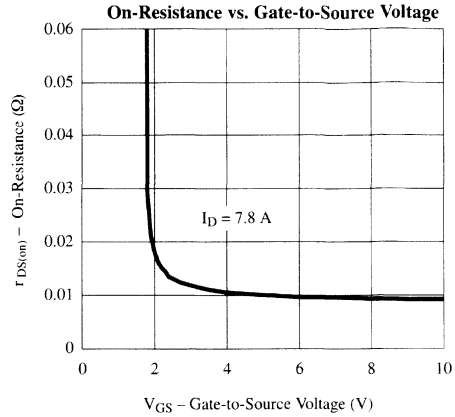
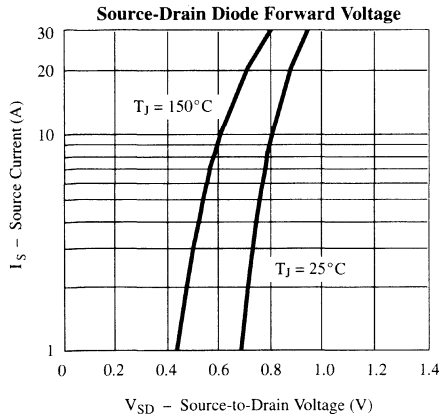
Typical Characteristics (25°C Unless Otherwise Noted)



2

TSSOP-8

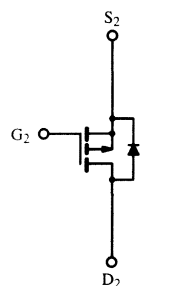
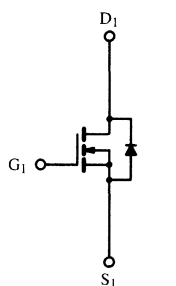
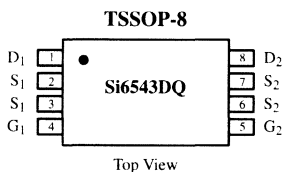
Typical Characteristics (25°C Unless Otherwise Noted)



Dual N- and P-Channel 30-V (D-S) Rated MOSFET

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.065 @ $V_{GS} = 10$ V	± 3.9
		0.095 @ $V_{GS} = 4.5$ V	± 3.1
P-Channel	-30	0.085 @ $V_{GS} = -10$ V	± 2.5
		0.19 @ $V_{GS} = -4.5$ V	± 1.8



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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	30	−30	V
Gate-Source Voltage		V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	± 3.9	± 2.5	A
	T _A = 70 °C		± 3.1	± 2.1	
Pulsed Drain Current		I _{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^a		I _S	1.25	−1.25	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	1.0		W
	T _A = 70 °C		0.64		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70181. A SPICE Model data sheet is available for this product (FaxBack document #70547).

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	N-Ch	1.0		V
		$V_{DS} = V_{GS}, I_D = -250\ \mu A$	P-Ch	-1.0		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V, V_{GS} = \pm 20\ V$	N-Ch P-Ch		± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ V, V_{GS} = 0\ V$	N-Ch		1	μA
		$V_{DS} = -30\ V, V_{GS} = 0\ V$	P-Ch		-1	
		$V_{DS} = 30\ V, V_{GS} = 0\ V, T_J = 55^\circ C$	N-Ch		25	
		$V_{DS} = -30\ V, V_{GS} = 0\ V, T_J = 55^\circ C$	P-Ch		-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ V, V_{GS} = 10\ V$	N-Ch	15		A
		$V_{DS} \geq -5\ V, V_{GS} = -10\ V$	P-Ch	-15		
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ V, I_D = 3.9\ A$	N-Ch		0.043	Ω
		$V_{GS} = -10\ V, I_D = 2.5\ A$	P-Ch		0.066	
		$V_{GS} = 4.5\ V, I_D = 3.1\ A$	N-Ch		0.075	
		$V_{GS} = -4.5\ V, I_D = 1.8\ A$	P-Ch		0.125	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ V, I_D = 3.9\ A$	N-Ch		7	S
		$V_{DS} = -15\ V, I_D = -2.5\ A$	P-Ch		5	
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ A, V_{GS} = 0\ V$	N-Ch		0.8	V
		$I_S = -1.25\ A, V_{GS} = 0\ V$	P-Ch		0.8	
Dynamic ^b						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\ V, V_{GS} = 10\ V, I_D = 3.9\ A$ P-Channel $V_{DS} = -10\ V, V_{GS} = -10\ V, I_D = -2.5\ A$	N-Ch		9.8	nC
Gate-Source Charge	Q_{gs}		P-Ch		8.7	
			N-Ch		2.1	
Gate-Drain Charge	Q_{gd}		P-Ch		1.9	
		N-Ch		1.6		
Turn-On Delay Time	$t_{d(on)}$	P-Ch		1.3		
		N-Ch		9		
Rise Time	t_r	P-Ch		7		
		N-Ch		15		
Turn-Off Delay Time	$t_{d(off)}$	N-Ch		6		
		P-Ch		18		
Fall Time	t_f	N-Ch		18		
		P-Ch		27		
Source-Drain Reverse Recovery Time	t_{rr}	N-Ch		14		
		P-Ch		27		
		N-Ch		6		
		P-Ch		15		
		N-Ch		8		
		P-Ch		15		
		N-Ch		48		
		P-Ch		80		
		N-Ch		46		
		P-Ch		80		

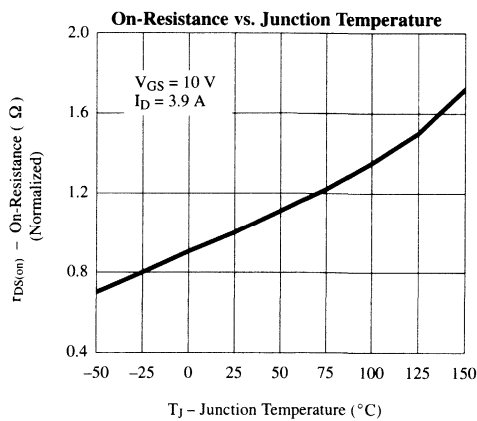
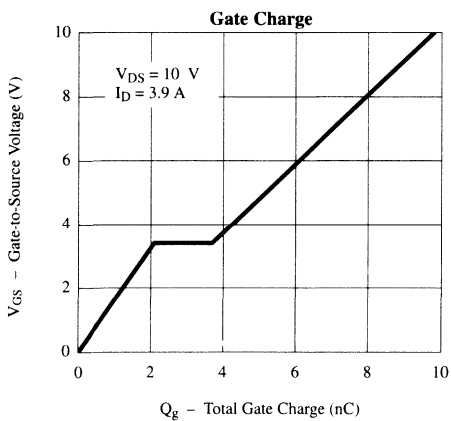
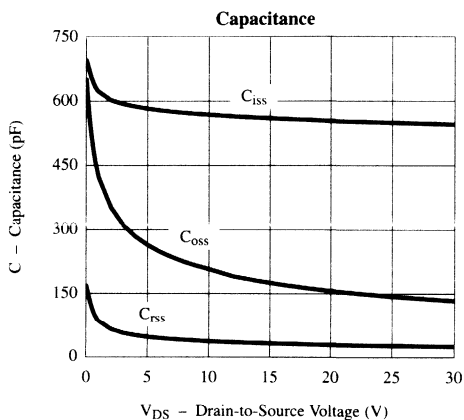
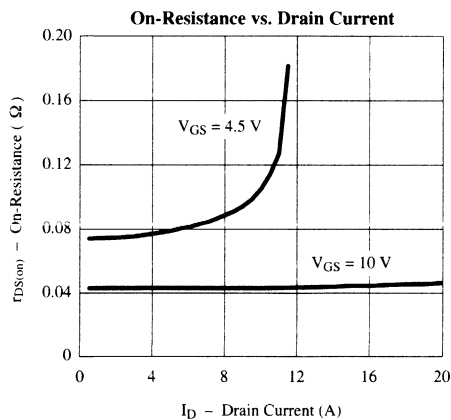
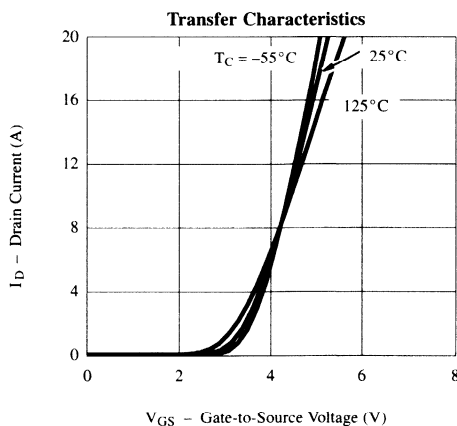
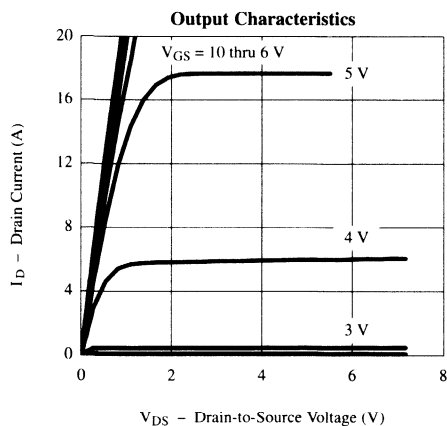
Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

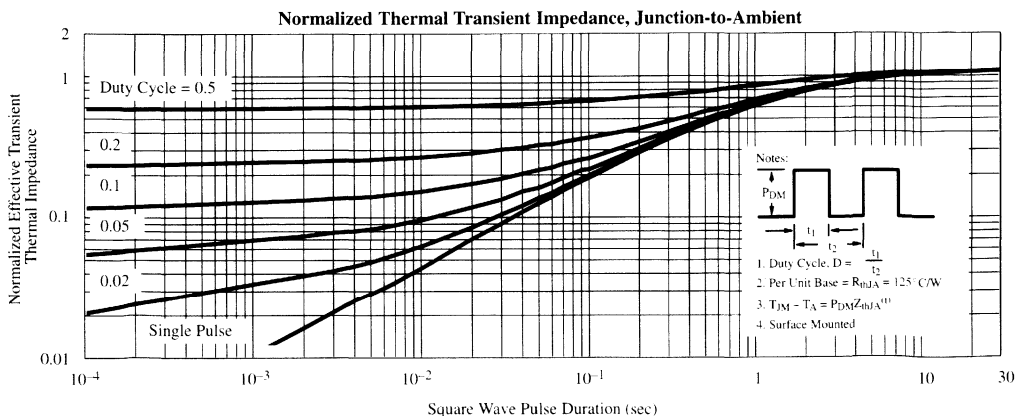
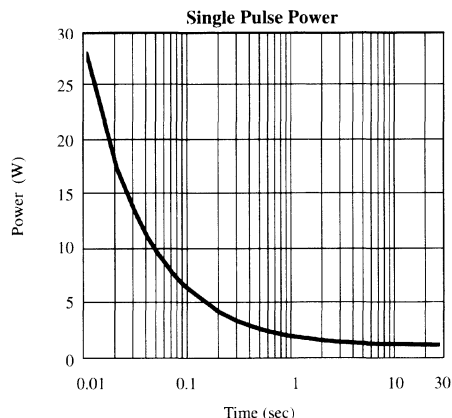
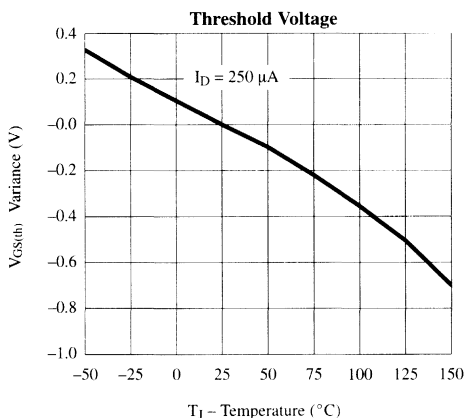
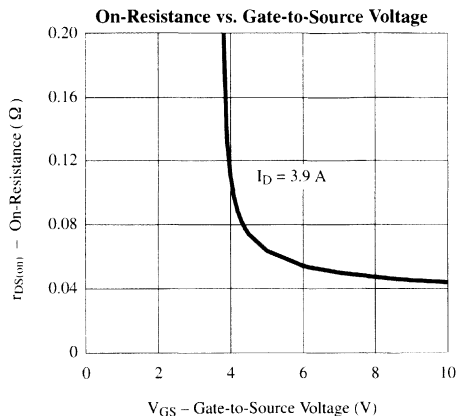
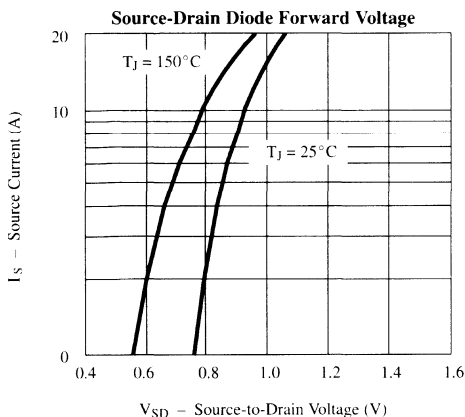
Typical Characteristics (25°C Unless Noted)

N-Channel



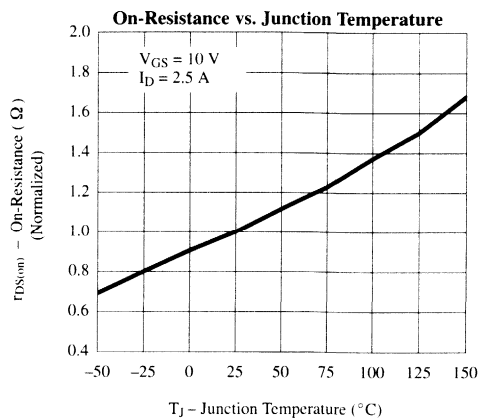
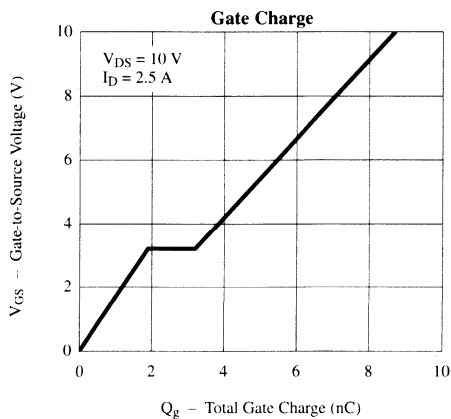
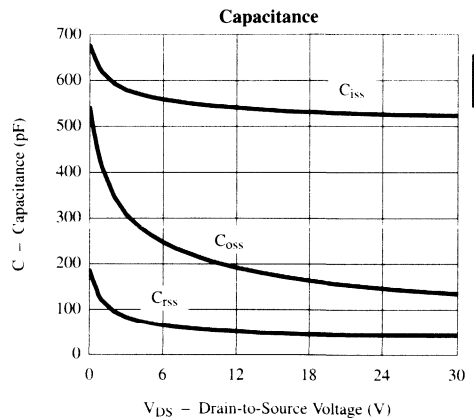
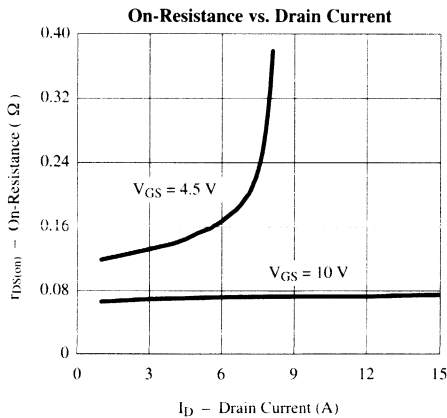
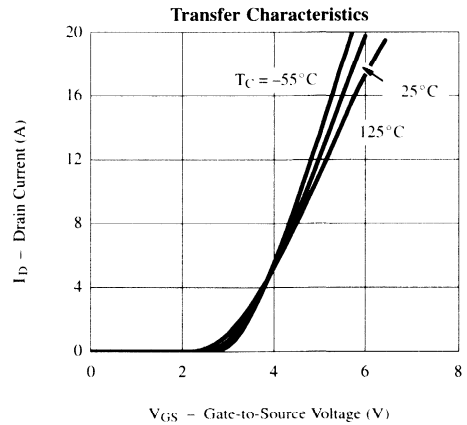
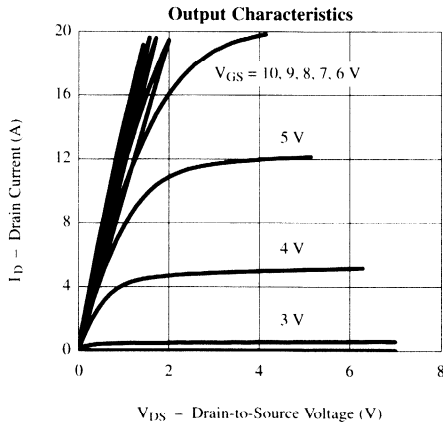
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TSSOP-8

Typical Characteristics (25°C Unless Noted)
N-Channel


Typical Characteristics (25°C Unless Noted)

P-Channel

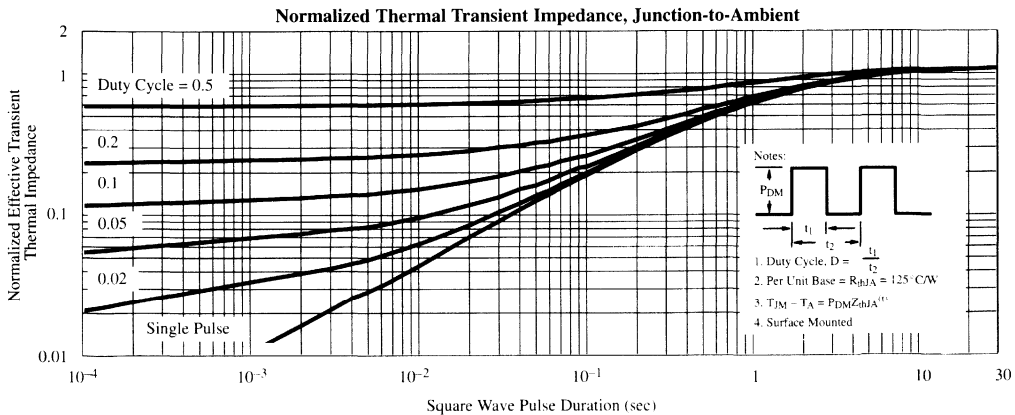
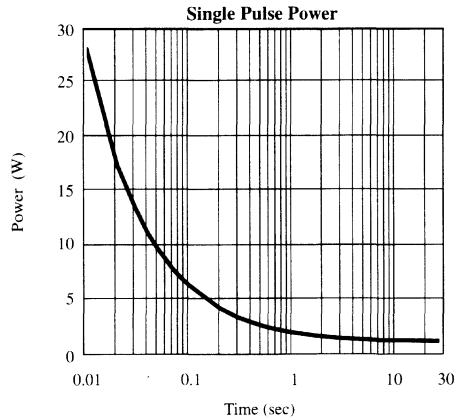
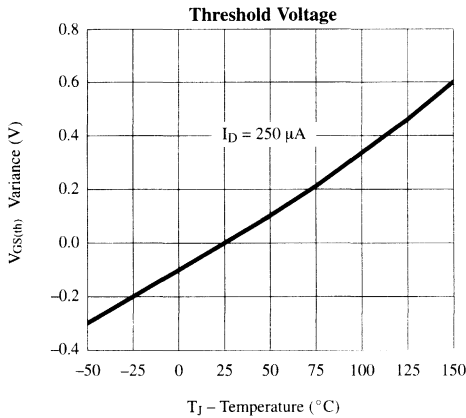
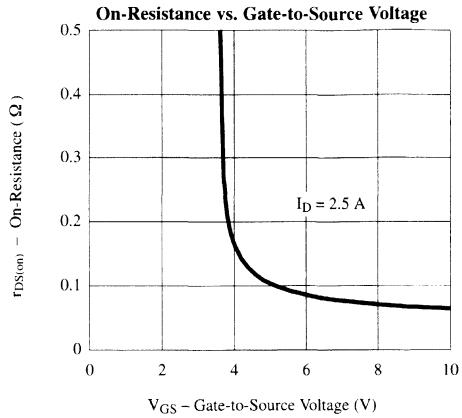
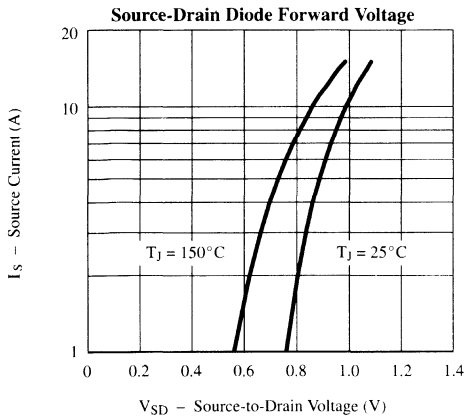


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TSSOP-8

Typical Characteristics (25°C Unless Noted)

P-Channel

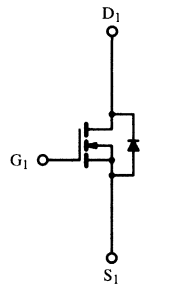
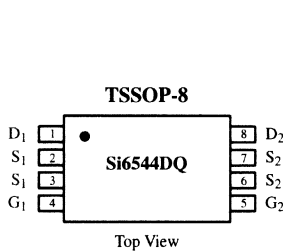


Dual N- and P-Channel 30-V (D-S) Rated MOSFET

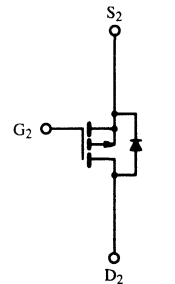
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.035 @ $V_{GS} = 10$ V	± 4.0
		0.050 @ $V_{GS} = 4.5$ V	± 3.4
P-Channel	-30	0.045 @ $V_{GS} = -10$ V	± 3.5
		0.090 @ $V_{GS} = -4.5$ V	± 2.5

TrenchFET™
Power MOSFETs



N-Channel MOSFET



P-Channel MOSFET

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TSSOP-8

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	30	−30	V
Gate-Source Voltage		V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 4.0	± 3.5	A
	T _A = 70°C		± 3.2	± 2.8	
Pulsed Drain Current		I _{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^a		I _S	1.25	−1.25	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	1.0		W
	T _A = 70°C		0.64		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70668.

Specifications (T_J = 25 °C Unless Otherwise Noted)

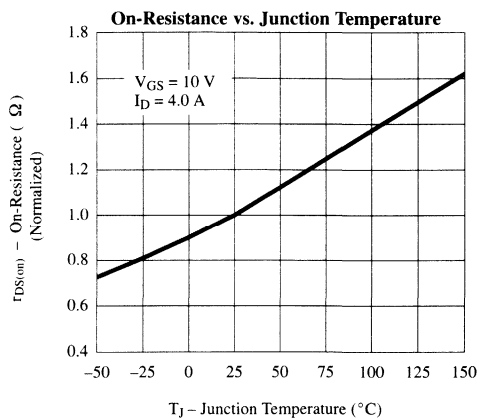
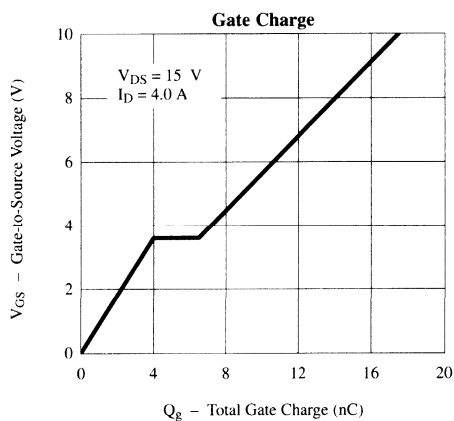
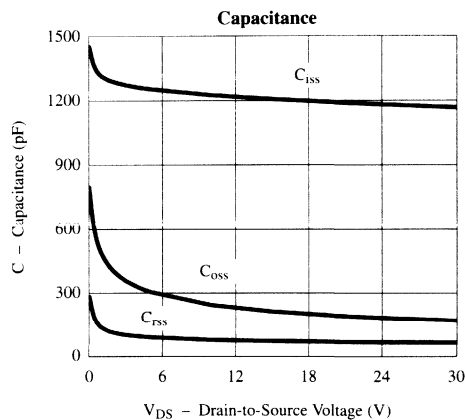
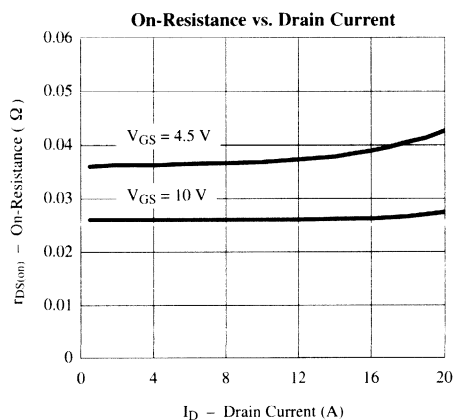
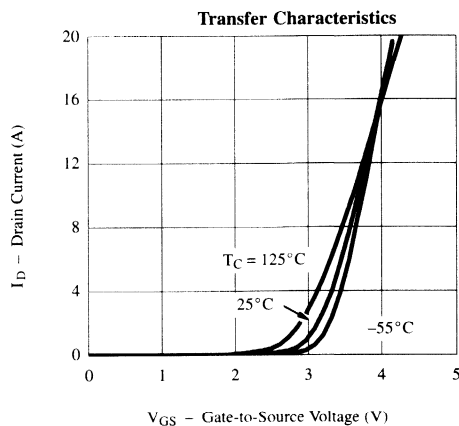
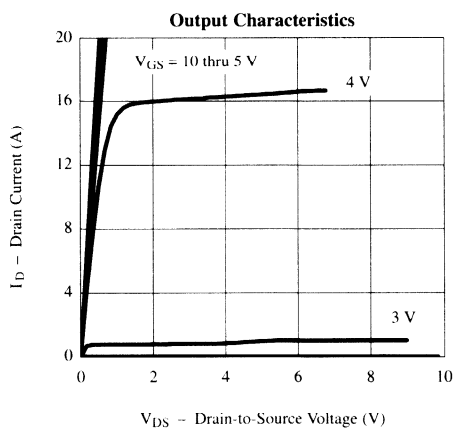
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit		
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0		V		
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0				
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch P-Ch		± 100 ± 100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch		1	μA		
		V _{DS} = -30 V, V _{GS} = 0 V	P-Ch		-1			
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch		5			
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch		-5			
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	20		A		
		V _{DS} ≥ -5 V, V _{GS} = -10 V	P-Ch	20				
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.0 A	N-Ch		0.027	Ω		
		V _{GS} = -10 V, I _D = 3.5 A	P-Ch		0.035			
		V _{GS} = 4.5 V, I _D = 3.4 A	N-Ch		0.038			
		V _{GS} = -4.5 V, I _D = 2.5 A	P-Ch		0.062			
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.0 A	N-Ch		13	S		
		V _{DS} = -15 V, I _D = -3.5 A	P-Ch		7.2			
Diode Forward Voltage ^a	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V	N-Ch		0.73	V		
		I _S = -1.25 A, V _{GS} = 0 V	P-Ch		-0.77			
Dynamic ^b								
Total Gate Charge	Q _g	N-Channel V _{DS} = 15 V, V _{GS} = 10 V, I _D = 4.0 A P-Channel V _{DS} = -15 V, V _{GS} = -10 V, I _D = -3.5 A	N-Ch P-Ch		17.5 17	30 30	nC	
Gate-Source Charge	Q _{gs}		N-Ch P-Ch		4.0 4.4			
			N-Ch P-Ch		2.5 3.1			
Gate-Drain Charge	Q _{gd}							
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	N-Ch P-Ch		12 13	20 20	ns	
Rise Time	t _r		N-Ch P-Ch		9 10	20 20		
			N-Ch P-Ch		25 33	50 60		
Turn-Off Delay Time	t _{d(off)}		N-Ch P-Ch		20 10	40 20		
Fall Time	t _f							
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.25 A, di/dt = 100 A/μs	N-Ch		25		60
		I _F = -1.25 A, di/dt = 100 A/μs	P-Ch		30	60		

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)

N-Channel

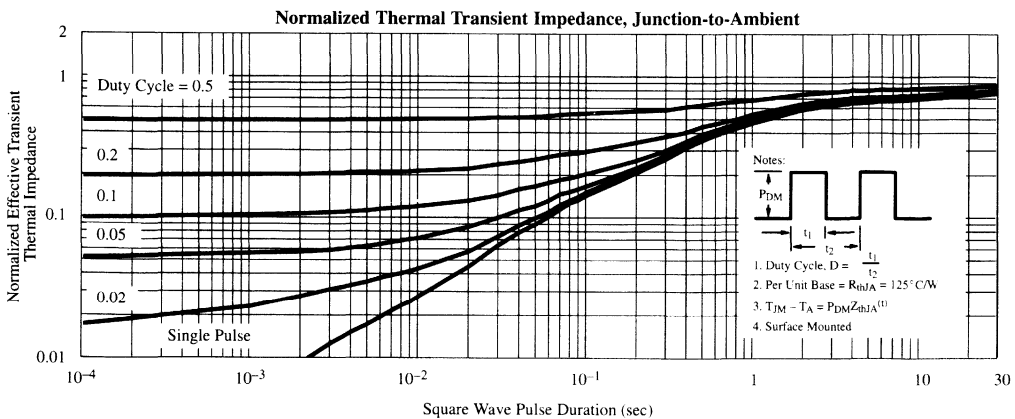
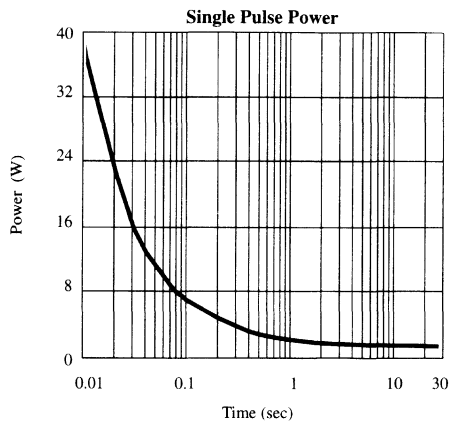
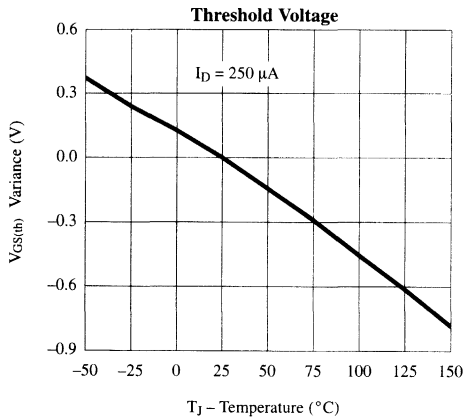
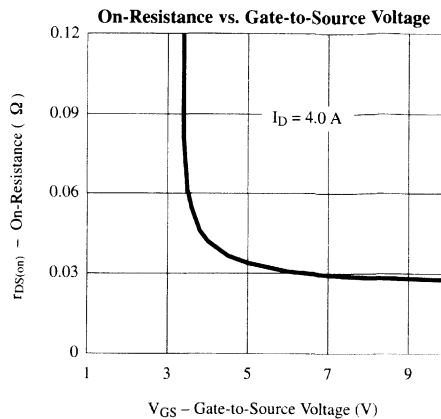
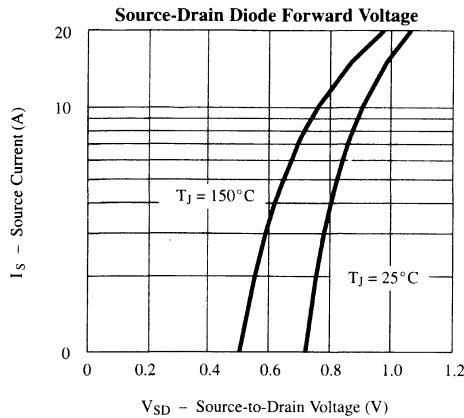


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TSSOP-8

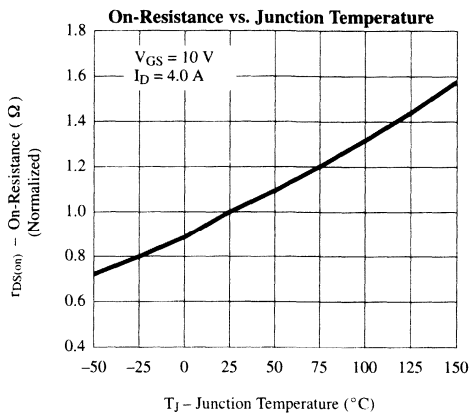
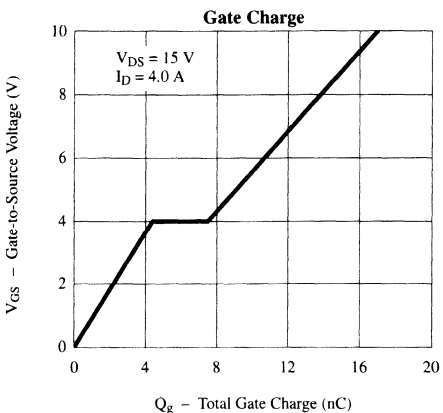
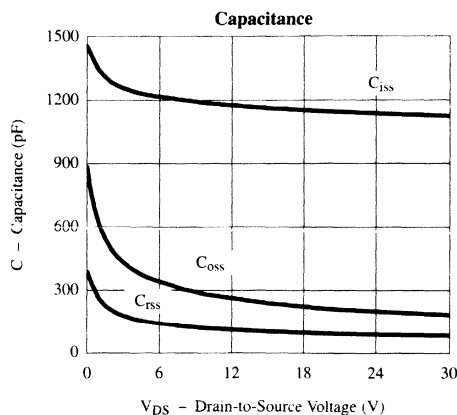
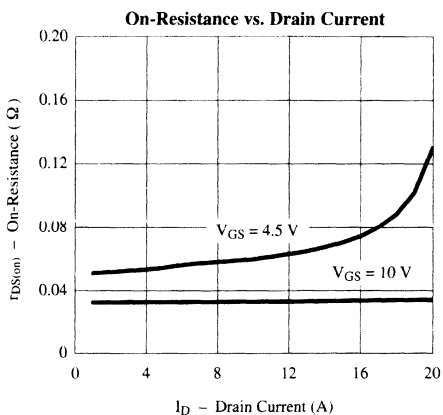
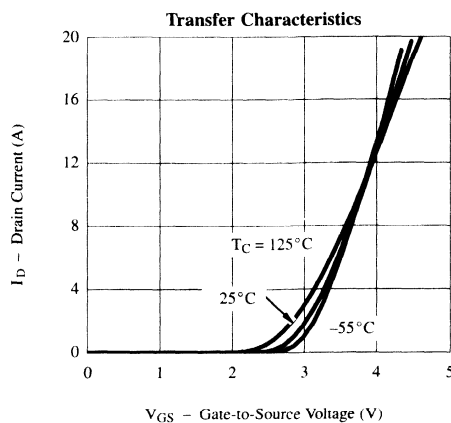
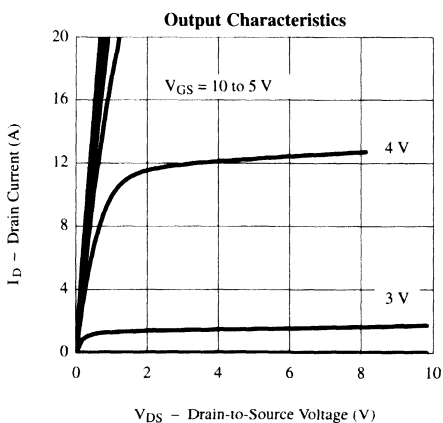
Typical Characteristics (25°C Unless Noted)

N-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

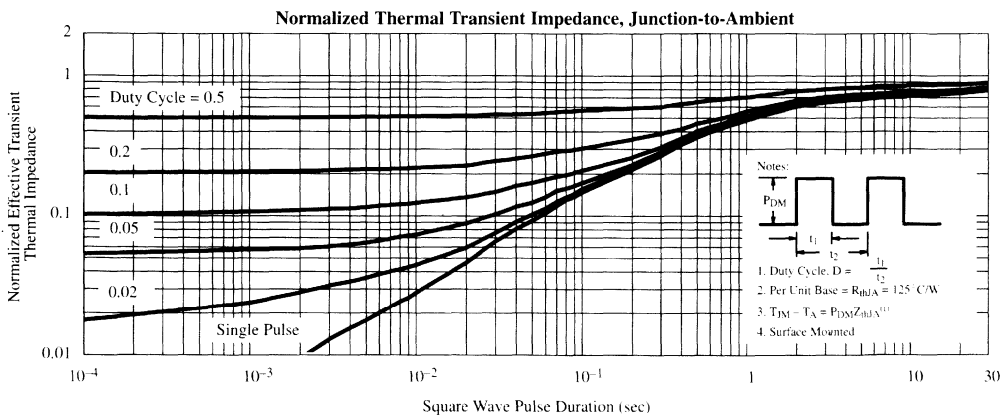
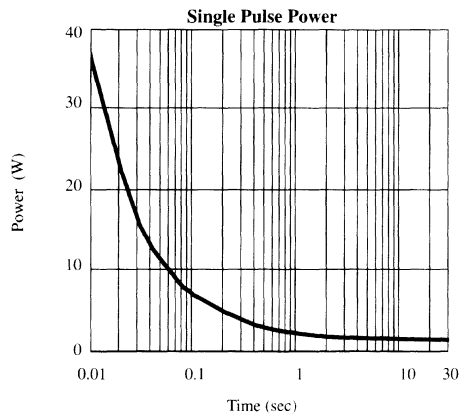
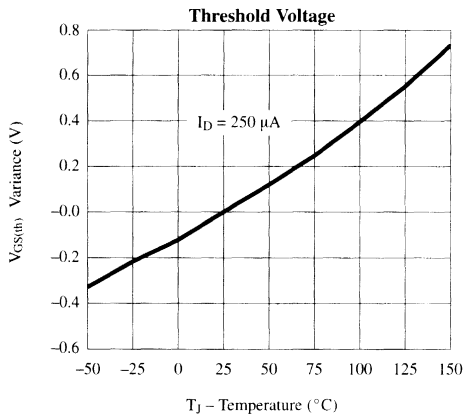
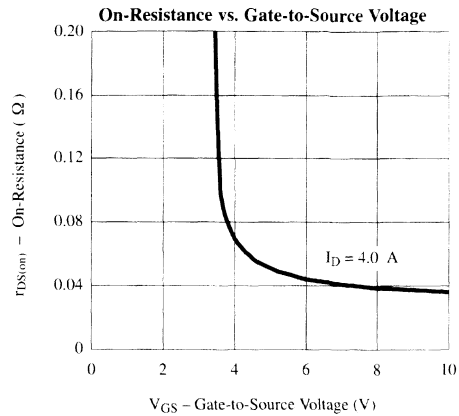
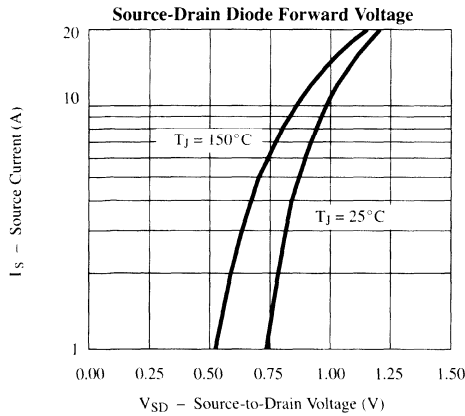


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TSSOP-8

Typical Characteristics (25°C Unless Noted)

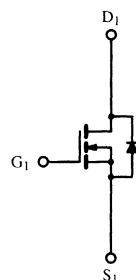
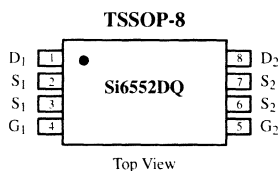
P-Channel



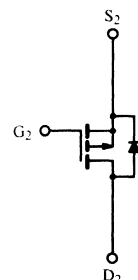
Dual N- and P-Channel 30-V (D-S) Rated MOSFET

Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.08 @ V _{GS} = 4.5 V	± 2.8
		0.11 @ V _{GS} = 2.5 V	± 2.1
P-Channel	-12	0.1 @ V _{GS} = -4.5 V	± 2.5
		0.18 @ V _{GS} = -2.5 V	± 1.9



N-Channel MOSFET



P-Channel MOSFET

2

TSSOP-8

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	-12	V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 2.8	± 2.5	A
	T _A = 70°C		± 2.3	± 2.0	
Pulsed Drain Current		I _{DM}	± 20		
Continuous Source Current (Diode Conduction) ^a		I _S	1.0	-1.0	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	1.0		W
	T _A = 70°C		0.64		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70175.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

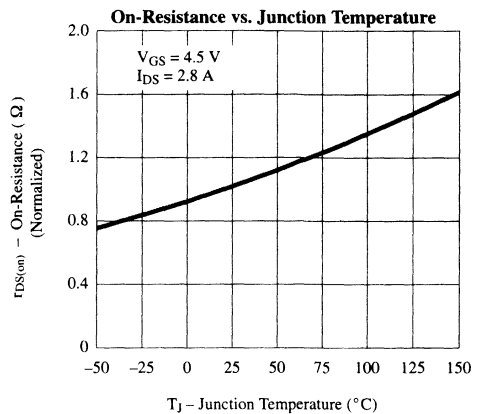
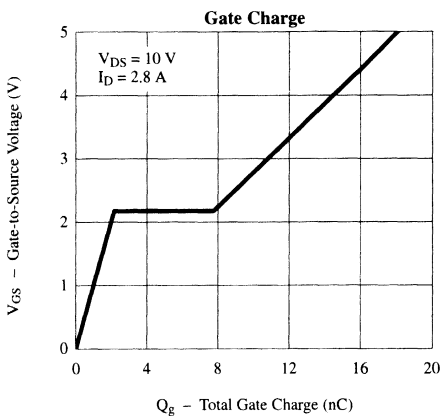
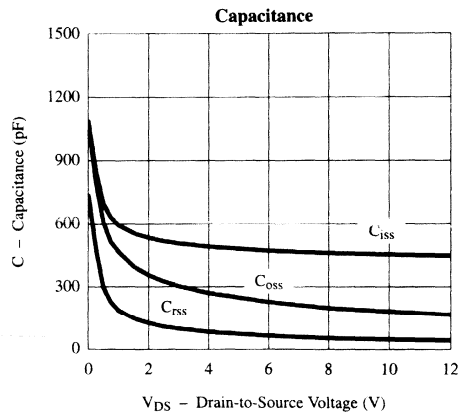
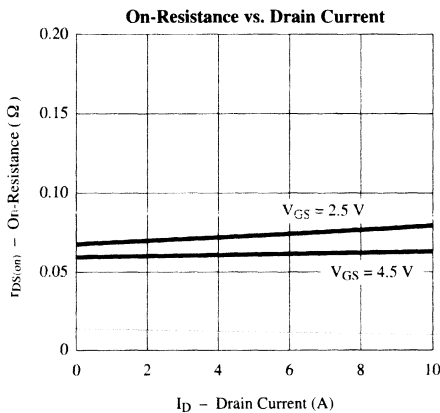
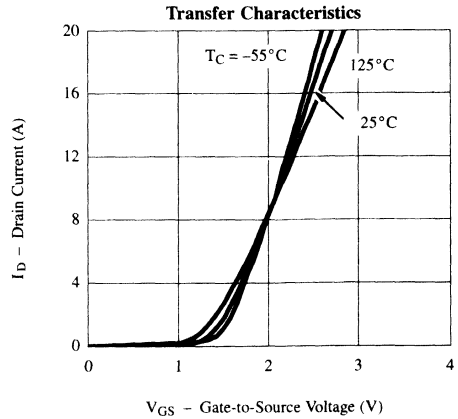
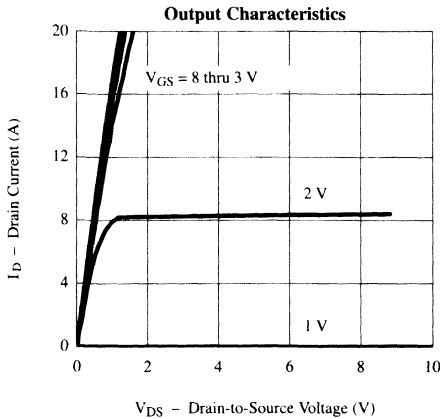
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	N-Ch	0.6		V
		$V_{DS} = V_{GS}, I_D = -250\ \mu A$	P-Ch	-0.6		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V, V_{GS} = \pm 8\ V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ V, V_{GS} = 0\ V$	N-Ch		1	μA
		$V_{DS} = -12\ V, V_{GS} = 0\ V$	P-Ch		-1	
		$V_{DS} = 20\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	N-Ch		5	
		$V_{DS} = -12\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	P-Ch		-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ V, V_{GS} = 4.5\ V$	N-Ch	10		A
		$V_{DS} = -5\ V, V_{GS} = -4.5\ V$	P-Ch	-10		
		$V_{DS} = 5\ V, V_{GS} = 2.5\ V$	N-Ch	4		
		$V_{DS} = -5\ V, V_{GS} = -2.5\ V$	P-Ch	-4		
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ V, I_D = 2.8\ A$	N-Ch		0.08	Ω
		$V_{GS} = -4.5\ V, I_D = 2.5\ A$	P-Ch		0.1	
		$V_{GS} = 2.5\ V, I_D = 2.1\ A$	N-Ch		0.11	
		$V_{GS} = -2.5\ V, I_D = 1.9\ A$	P-Ch		0.18	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ V, I_D = 2.8\ A$	N-Ch		12	S
		$V_{DS} = -9\ V, I_D = -2.5\ A$	P-Ch		7	
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.0\ A, V_{GS} = 0\ V$	N-Ch		1.2	V
		$I_S = -1.0\ A, V_{GS} = 0\ V$	P-Ch		-1.2	
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ V, V_{GS} = 4.5\ V, I_D = 2.8\ A$ $V_{DS} = -6\ V, V_{GS} = -4.5\ V, I_D = -2.5\ A$	N-Ch		16	nC
Gate-Source Charge	Q_{gs}		P-Ch		9	
			N-Ch		3	
Gate-Drain Charge	Q_{gd}		P-Ch		2	
		N-Ch		6		
Turn-On Delay Time	$t_{d(on)}$	P-Ch		3		
		N-Ch		37		
Rise Time	t_r	P-Ch		21		
		N-Ch		66		
Turn-Off Delay Time	$t_{d(off)}$	P-Ch		35		
		N-Ch		56		
Fall Time	t_f	P-Ch		43		
		N-Ch		57		
Source-Drain Reverse Recovery Time	t_{rr}	P-Ch		22		
		N-Ch		26		
		P-Ch		35	70	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)

N-Channel

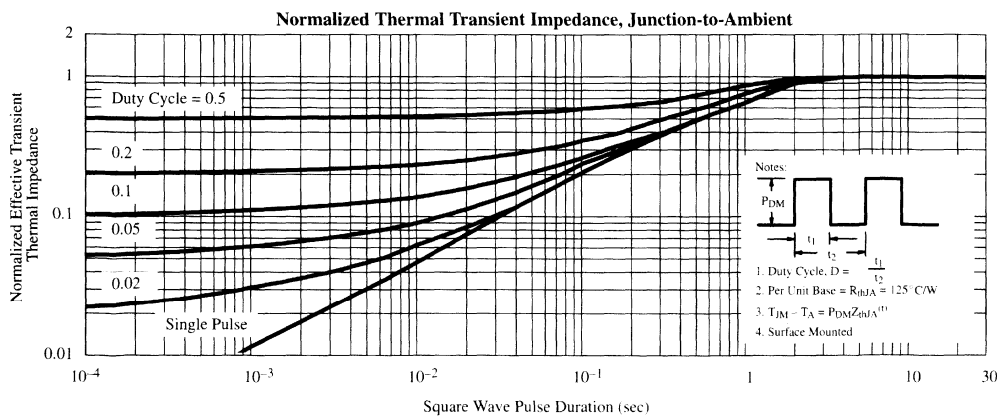
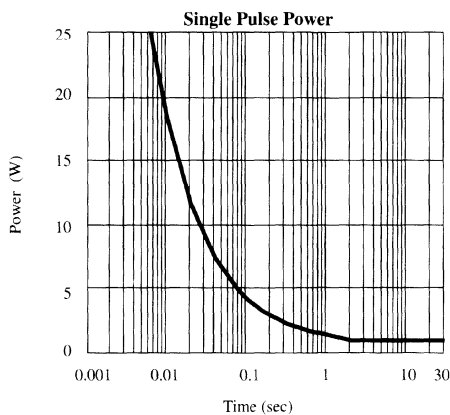
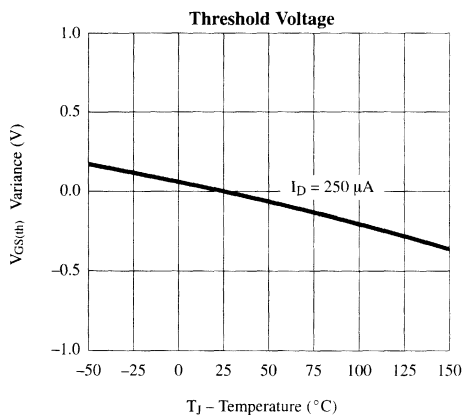
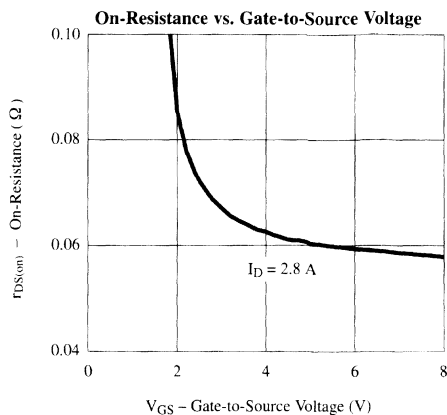
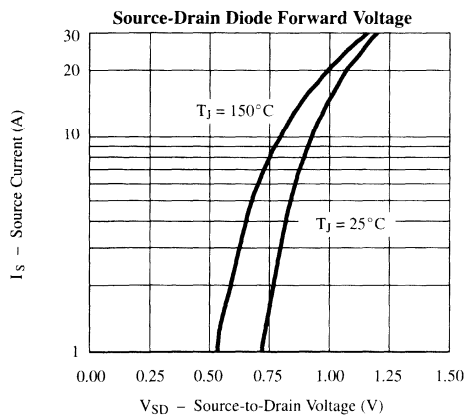


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TSSOP-8

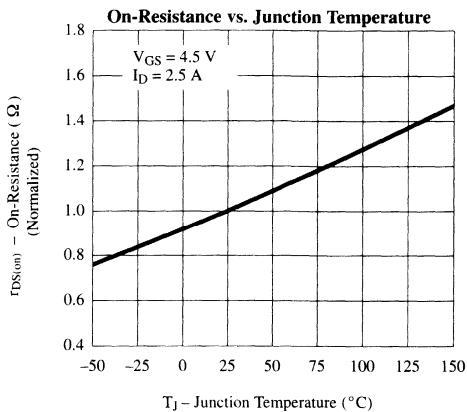
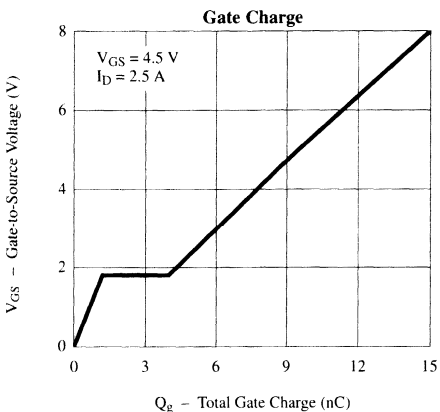
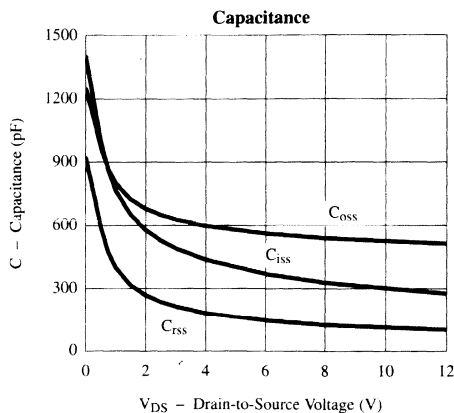
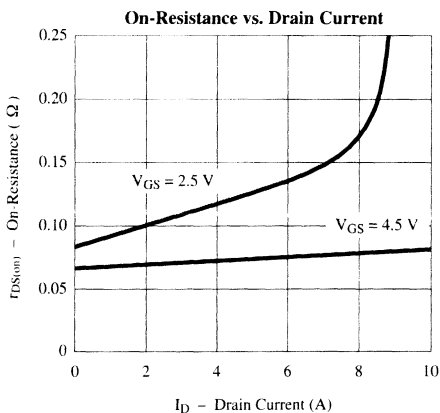
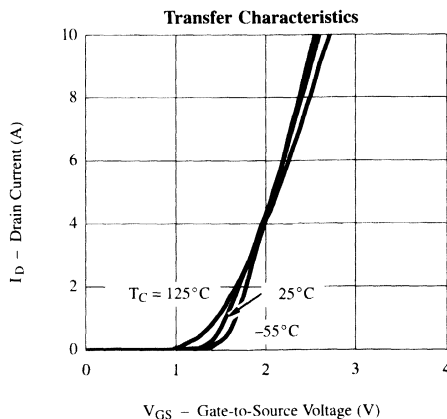
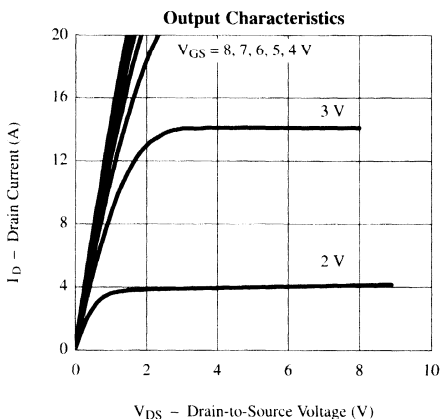
Typical Characteristics (25°C Unless Noted)

N-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

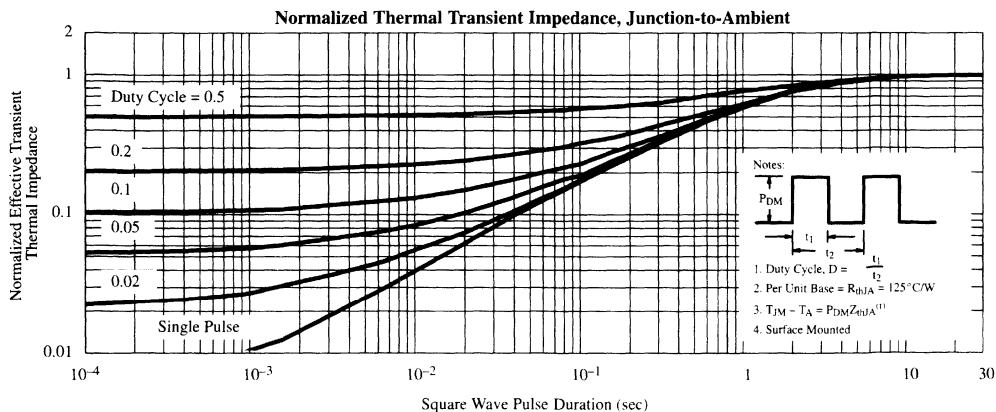
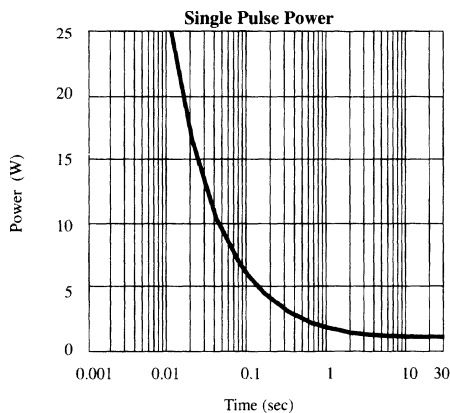
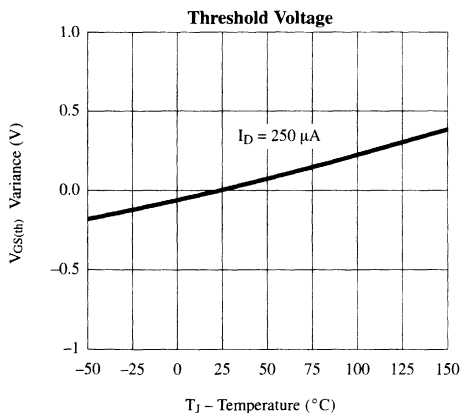
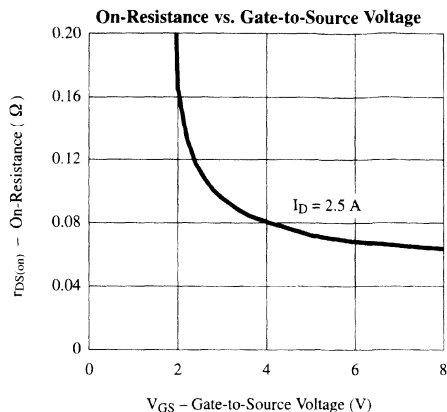
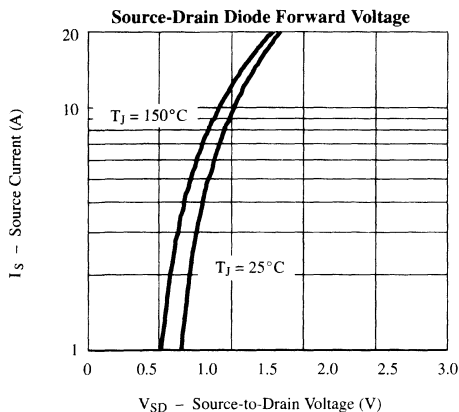


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TSSOP-8

Typical Characteristics (25°C Unless Noted)

P-Channel

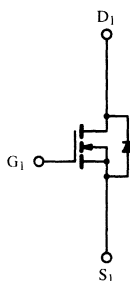
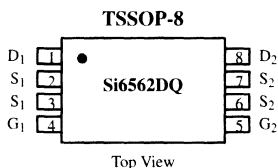


Dual N- and P-Channel 2.5-V (G-S) Rated MOSFET

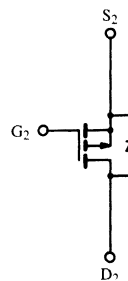
Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.030 @ V _{GS} = 4.5 V	± 4.5
		0.040 @ V _{GS} = 2.5 V	± 3.9
P-Channel	-20	0.050 @ V _{GS} = -4.5 V	± 3.5
		0.085 @ V _{GS} = -2.5 V	± 2.7

TrenchFET™
Power MOSFETs
2.5-V Rated



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	−20	V
Gate-Source Voltage		V _{GS}	± 12	± 12	
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 4.5	± 3.5	A
	T _A = 70°C		± 3.6	± 2.7	
Pulsed Drain Current		I _{DM}	± 30	± 30	
Continuous Source Current (Diode Conduction) ^a		I _S	1.25	−1.25	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	1.0		W
	T _A = 70°C		0.64		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70720.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

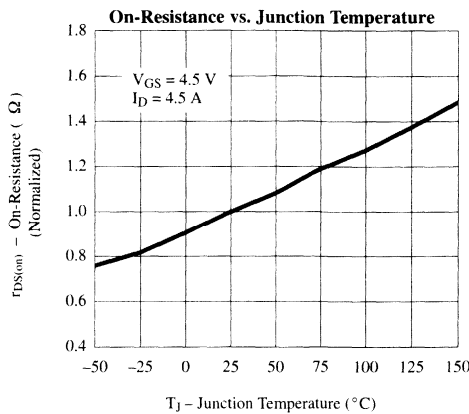
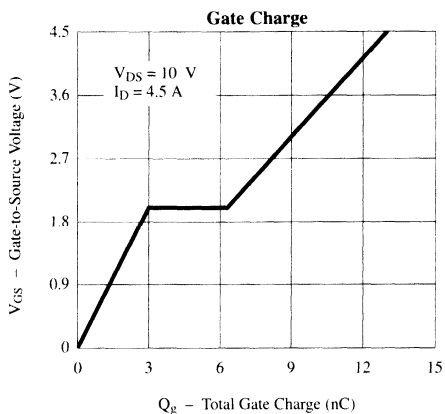
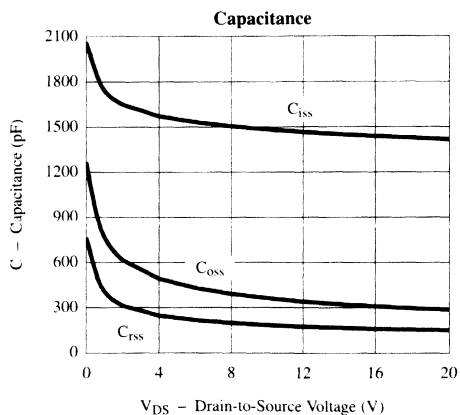
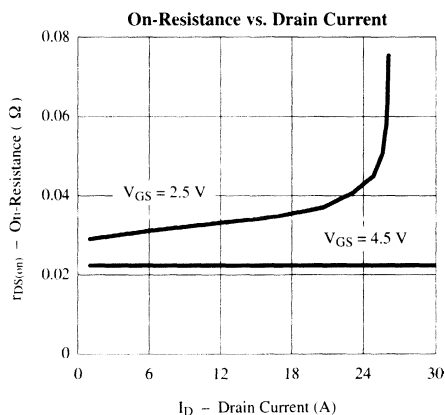
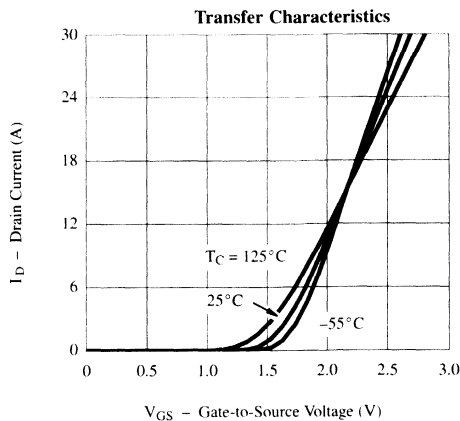
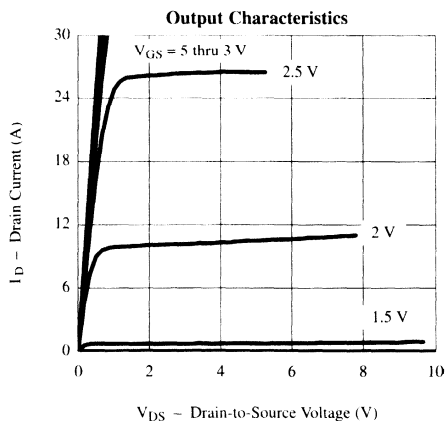
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	N-Ch	0.6		V	
		$V_{DS} = V_{GS}, I_D = -250\ \mu A$	P-Ch	-0.6			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V, V_{GS} = \pm 12\ V$	N-Ch P-Ch		± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ V, V_{GS} = 0\ V$	N-Ch		1	μA	
		$V_{DS} = -20\ V, V_{GS} = 0\ V$	P-Ch		-1		
		$V_{DS} = 20\ V, V_{GS} = 0\ V, T_J = 55^\circ C$	N-Ch		25		
		$V_{DS} = -20\ V, V_{GS} = 0\ V, T_J = 55^\circ C$	P-Ch		-25		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ V, V_{GS} = 4.5\ V$	N-Ch	30		A	
		$V_{DS} \geq -5\ V, V_{GS} = -4.5\ V$	P-Ch	-30			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ V, I_D = 4.5\ A$	N-Ch		0.023	0.030	Ω
		$V_{GS} = -4.5\ V, I_D = 3.5\ A$	P-Ch		0.040	0.050	
		$V_{GS} = 2.5\ V, I_D = 3.9\ A$	N-Ch		0.030	0.040	
		$V_{GS} = -2.5\ V, I_D = 2.7\ A$	P-Ch		0.060	0.085	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ V, I_D = 4.5\ A$	N-Ch		20	S	
		$V_{DS} = -10\ V, I_D = -3.5\ A$	P-Ch		10		
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ A, V_{GS} = 0\ V$	N-Ch		0.65	1.2	V
		$I_S = -1.25\ A, V_{GS} = 0\ V$	P-Ch		0.72	-1.2	
Dynamic ^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 15\ V, V_{GS} = 4.5\ V, I_D = 4.5\ A$ P-Channel $V_{DS} = -15\ V, V_{GS} = -4.5\ V, I_D = -3.5\ A$	N-Ch		13	25	nC
Gate-Source Charge	Q_{gs}		P-Ch		14.5	25	
			N-Ch		3.0		
Gate-Drain Charge	Q_{gd}		P-Ch		3.5		
		N-Ch		3.3			
Turn-On Delay Time	$t_{d(on)}$	P-Ch		3.5			
		N-Ch		22	50		
Rise Time	t_r	P-Ch		27	50		
		N-Ch		40	80		
		P-Ch		30	60		
Turn-Off Delay Time	$t_{d(off)}$	N-Ch		50	100	ns	
		P-Ch		57	100		
Fall Time	t_f	N-Ch		20	40		
		P-Ch		21	40		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\ A, di/dt = 100\ A/\mu s$	N-Ch		30	60	
		$I_F = -1.25\ A, di/dt = 100\ A/\mu s$	P-Ch		60	100	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)

N-Channel

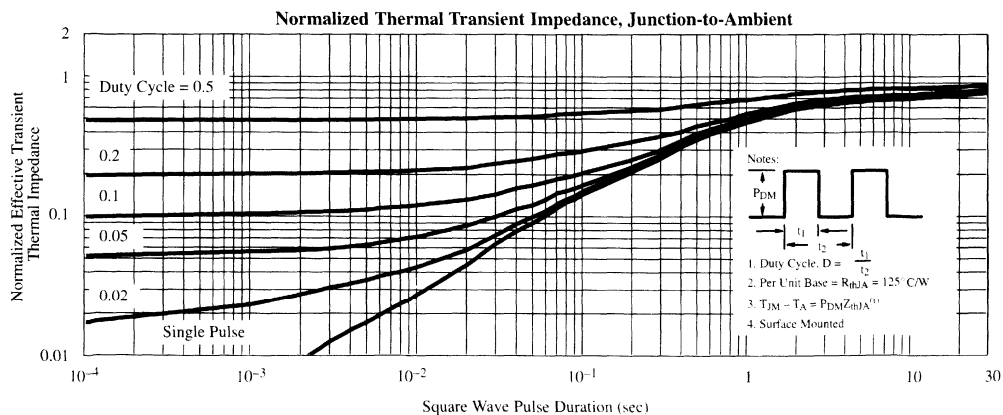
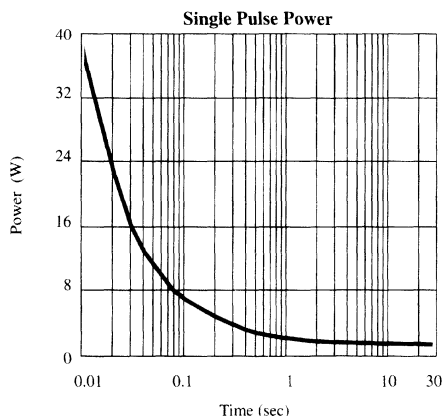
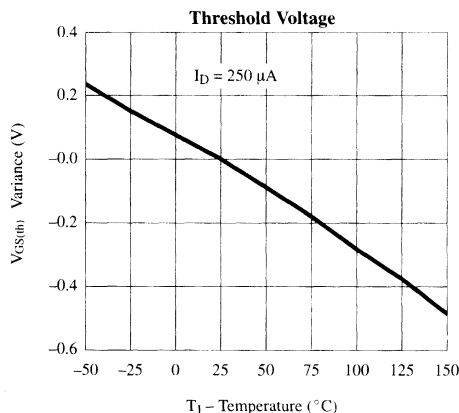
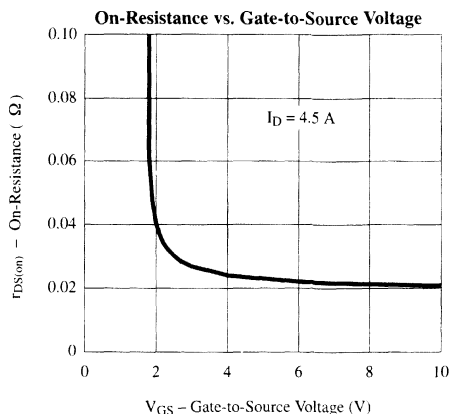
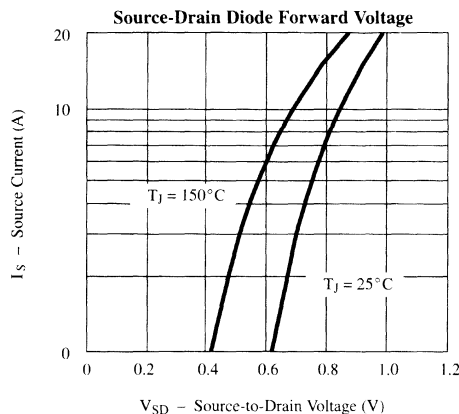


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TSSOP-8

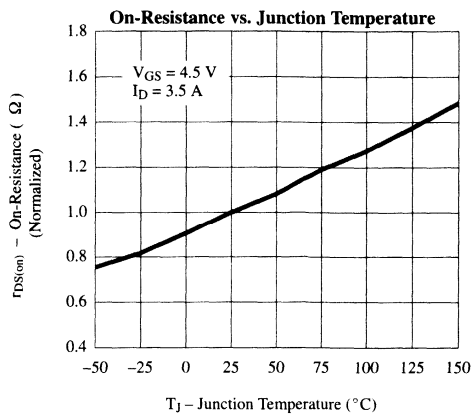
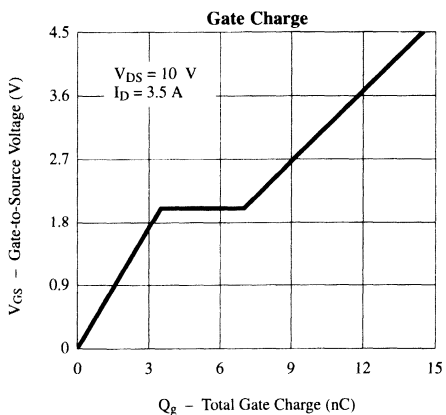
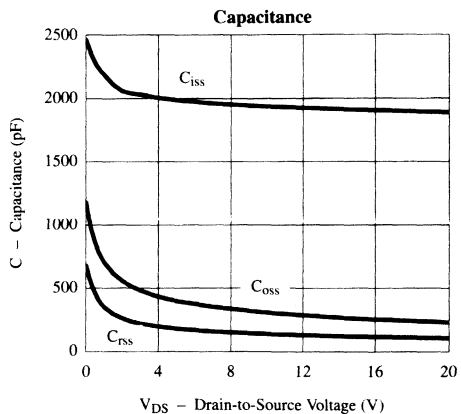
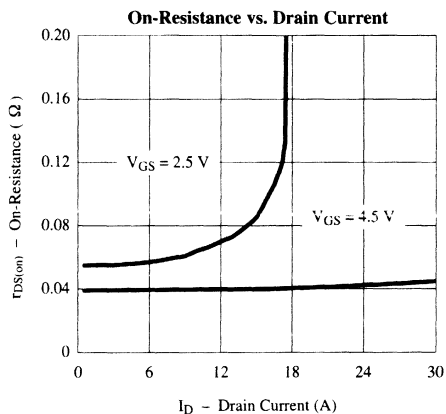
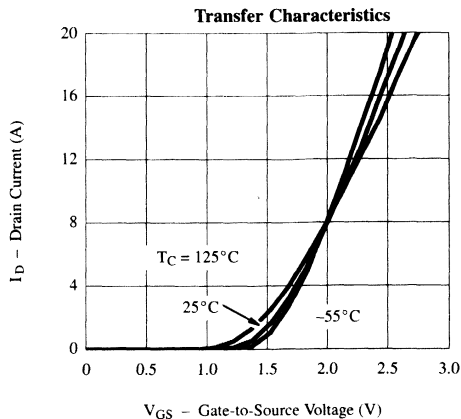
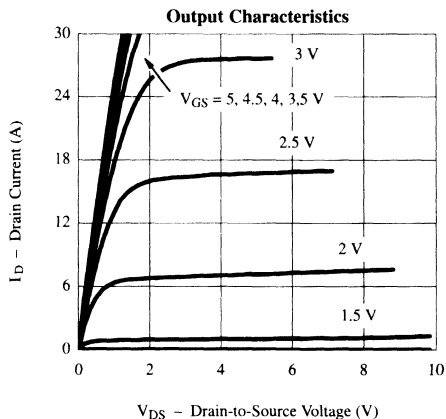
Typical Characteristics (25°C Unless Noted)

N-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

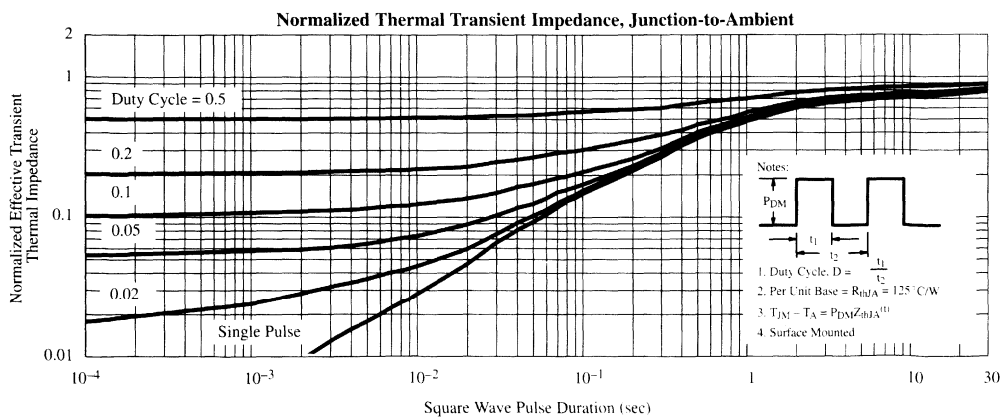
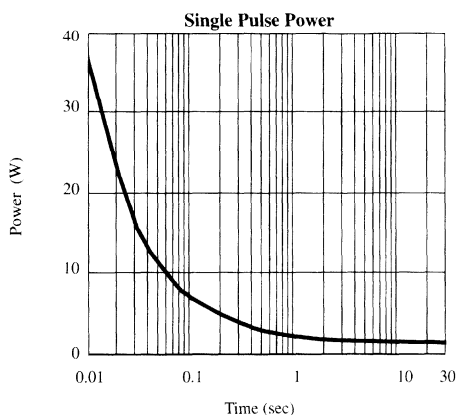
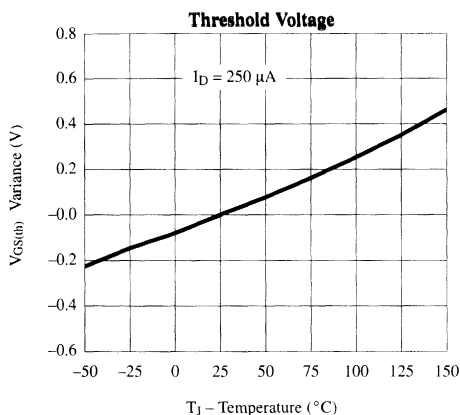
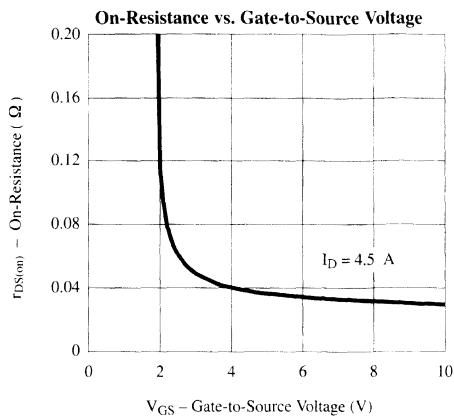
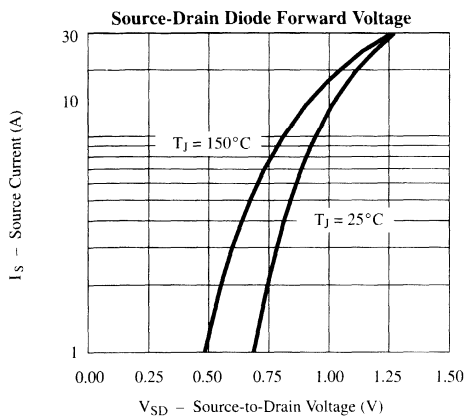


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Typical Characteristics (25°C Unless Noted)

P-Channel

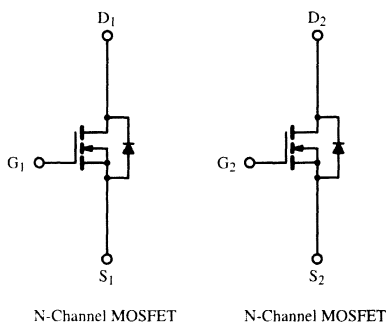
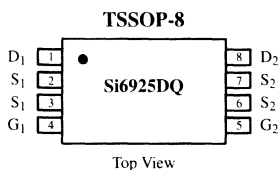


Dual N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.05 @ $V_{GS} = 4.5$ V	± 3.4
	0.06 @ $V_{GS} = 3.0$ V	± 3.1
	0.08 @ $V_{GS} = 2.5$ V	± 2.7

2.5-V Rated



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 3.4	A
		± 2.7	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I_S	1.25	W
Maximum Power Dissipation ^a	P_D	1	
		0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70631.

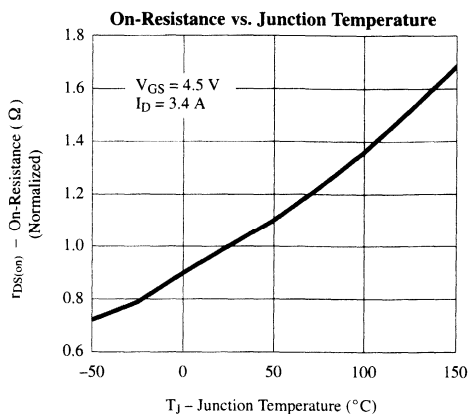
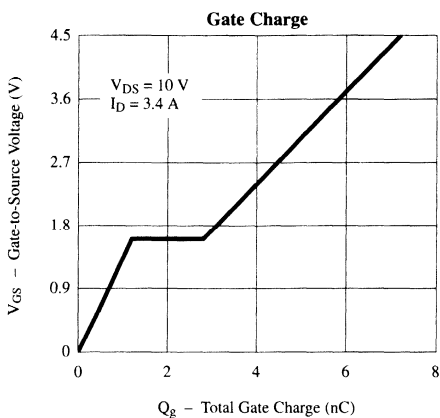
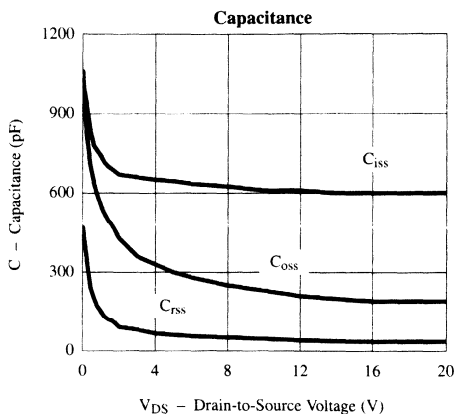
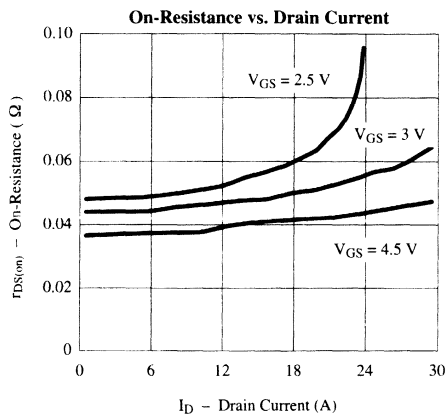
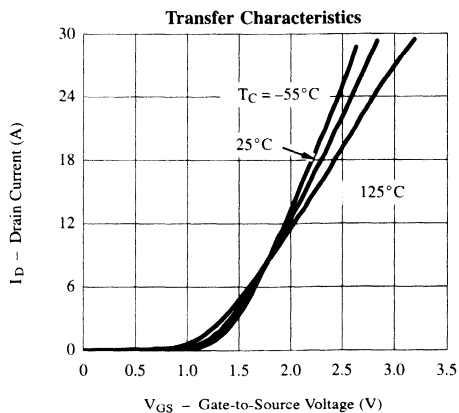
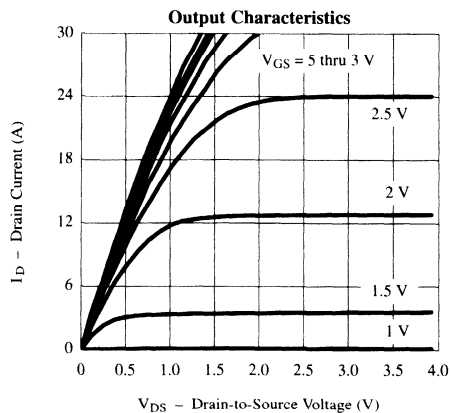
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.5			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 70°C			5	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	10			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 3.4 A		0.038	0.05	Ω
		V _{GS} = 3.0 V, I _D = 3.1 A		0.044	0.07	
		V _{GS} = 2.5 V, I _D = 2.7 A		0.048	0.08	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 3.4 A		18		S
Diode Forward Voltage ^b	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V		0.7	1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 3.4 A		7.5	15	nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			1.8		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 6 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		10	20	ns
Rise Time	t _r			25	50	
Turn-Off Delay Time	t _{d(off)}			40	60	
Fall Time	t _f			10	20	
Source-Drain Reverse Recovery Time	t _{rr}			50	90	

Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

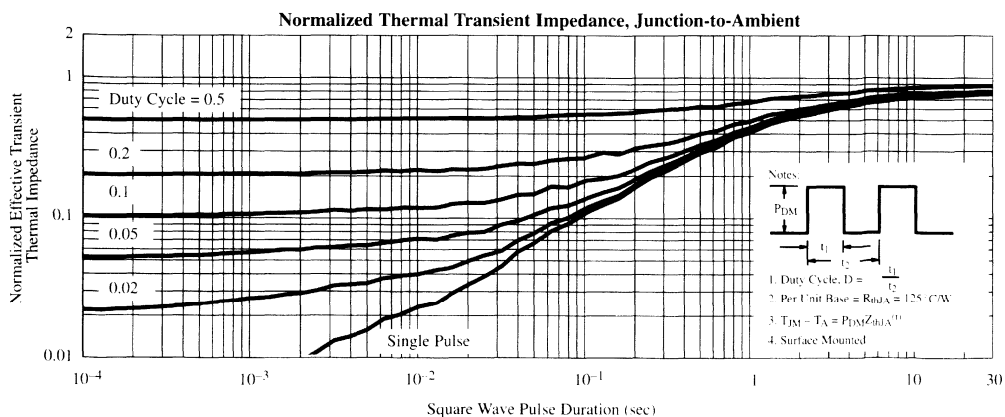
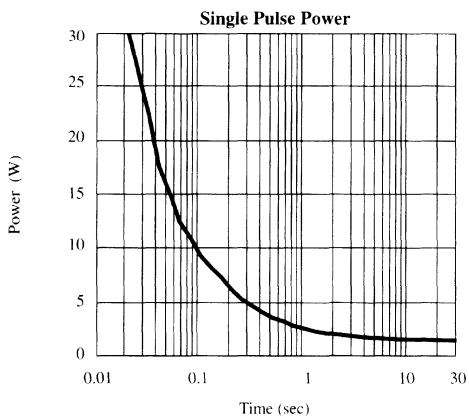
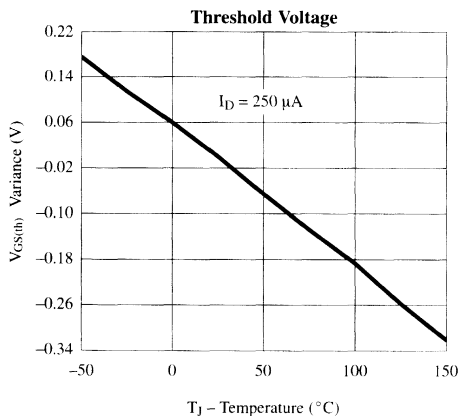
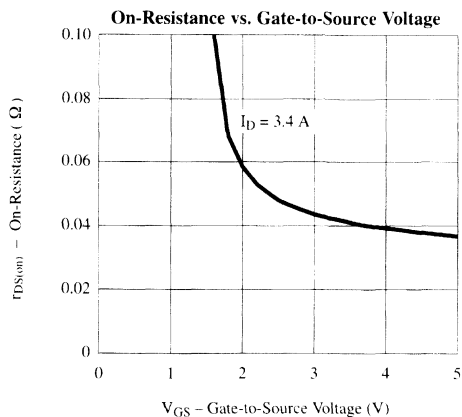
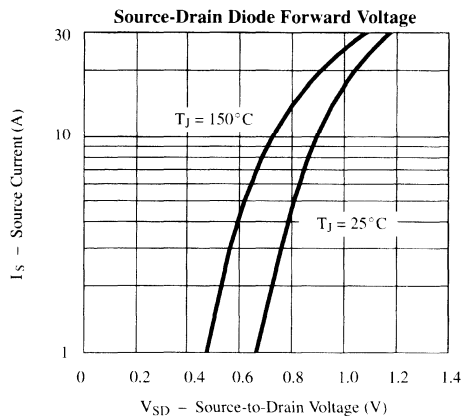
Typical Characteristics (25°C Unless Otherwise Noted)



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Typical Characteristics (25°C Unless Otherwise Noted)

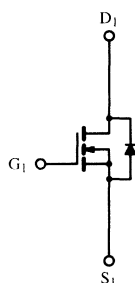
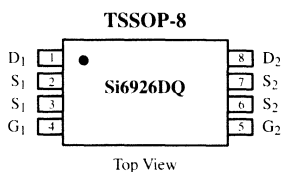


Dual N-Channel 2.5-V (G-S) Rated MOSFET

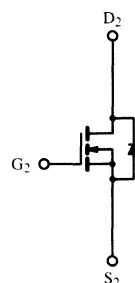
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.035 @ $V_{GS} = 4.5$ V	± 4.0
	0.040 @ $V_{GS} = 3.0$ V	± 3.7
	0.045 @ $V_{GS} = 2.5$ V	± 3.5

TrenchFET™
Power MOSFETs
2.5-V Rated



N-Channel MOSFET



N-Channel MOSFET

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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 4.0	A
		± 3.2	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	1.25	
Maximum Power Dissipation ^a	P_D	1.0	W
		0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70624.

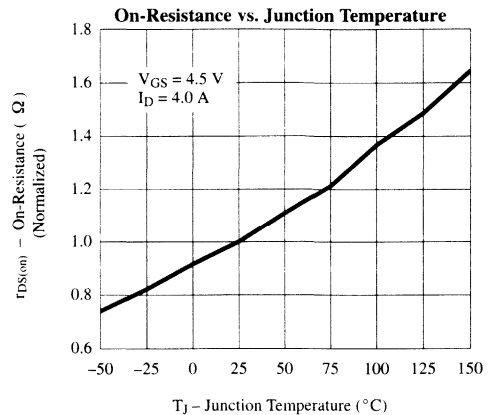
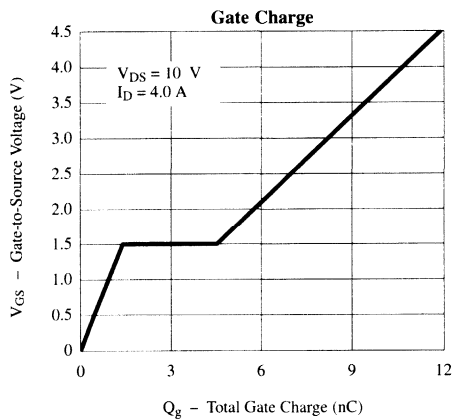
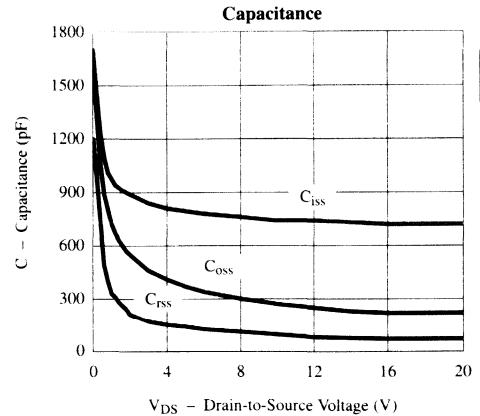
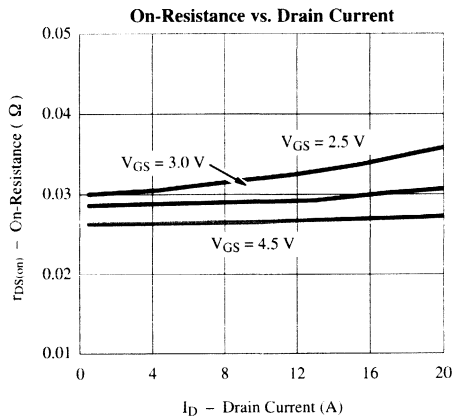
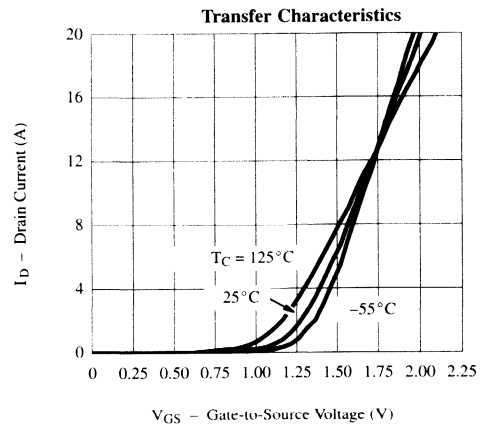
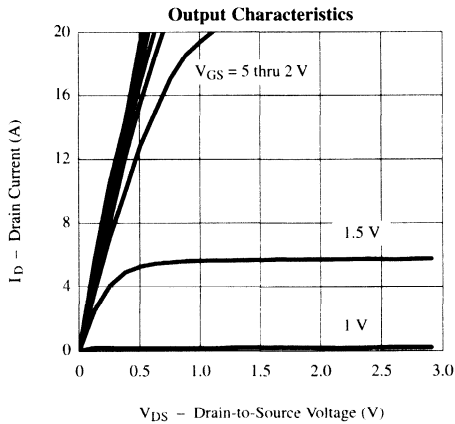
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.5			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 5\ \text{V}$	10			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 4.0\ \text{A}$		0.028	0.035	Ω
		$V_{GS} = 3.0\ \text{V}, I_D = 3.7\ \text{A}$		0.031	0.040	
		$V_{GS} = 2.5\ \text{V}, I_D = 3.5\ \text{A}$		0.033	0.045	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 4.0\ \text{A}$		18		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ \text{A}, V_{GS} = 0\ \text{V}$		0.7	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 4.0\ \text{A}$		12	20	nC
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			3.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 6\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			30	50	
Turn-Off Delay Time	$t_{d(off)}$			60	80	
Fall Time	t_f			15	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	90	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

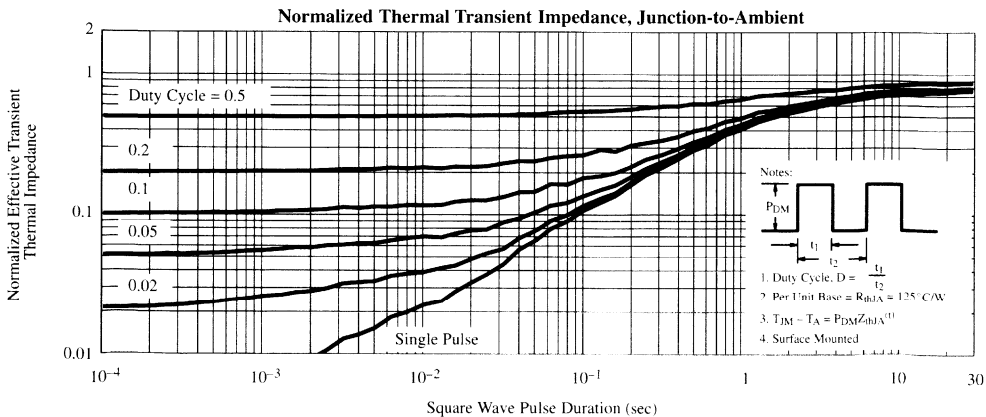
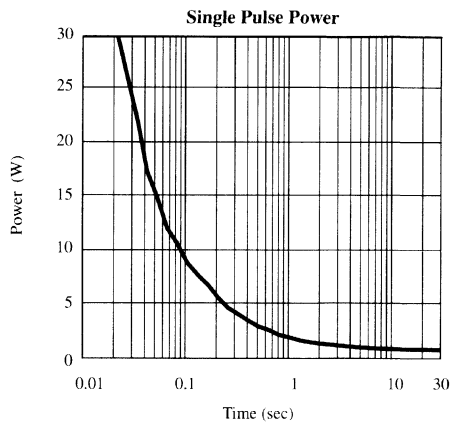
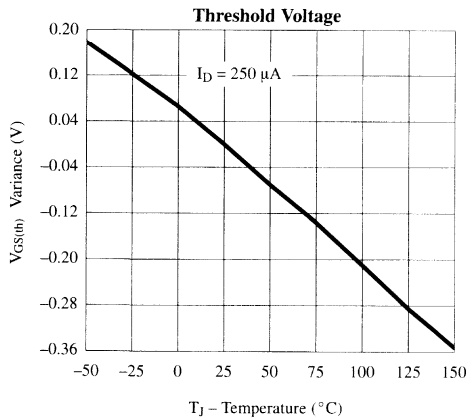
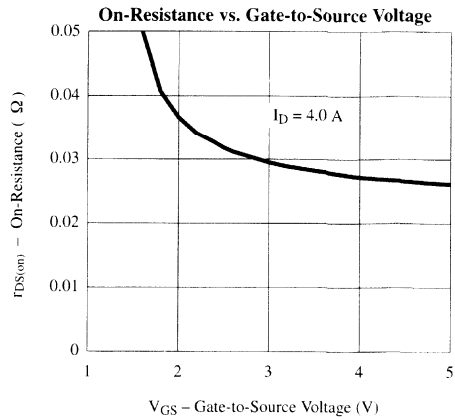
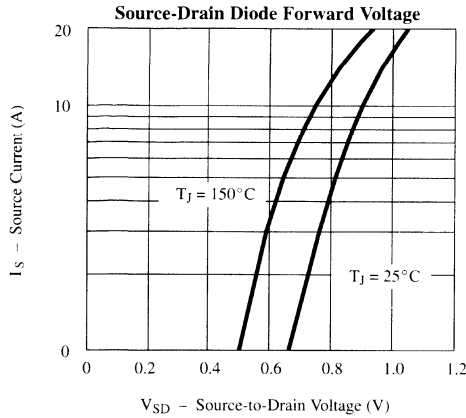
Typical Characteristics (25°C Unless Otherwise Noted)



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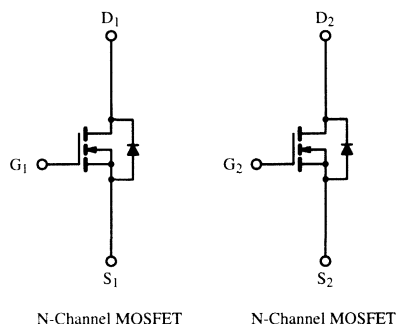
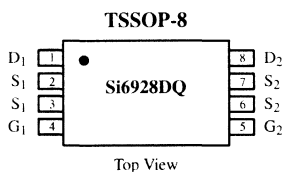
Typical Characteristics (25°C Unless Otherwise Noted)



Dual N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.035 @ $V_{GS} = 10$ V	± 4.0
	0.050 @ $V_{GS} = 4.5$ V	± 3.4



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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 4.0	A
		± 3.2	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	1.25	W
Maximum Power Dissipation ^a	P_D	1.0	
		0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70663.

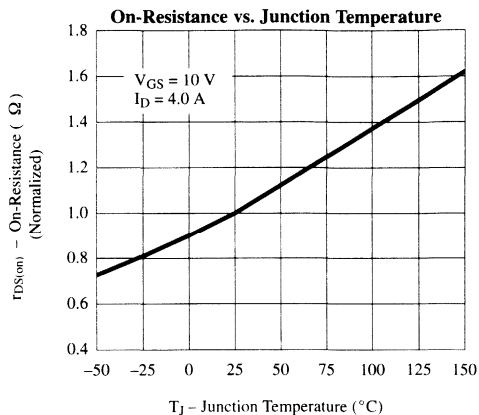
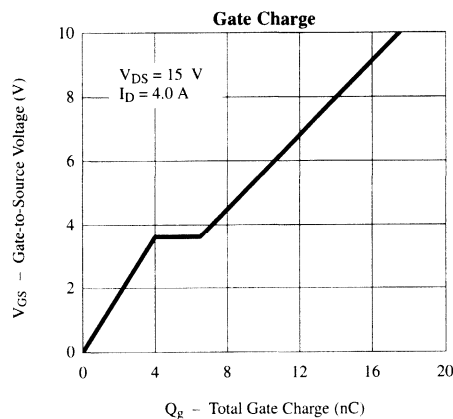
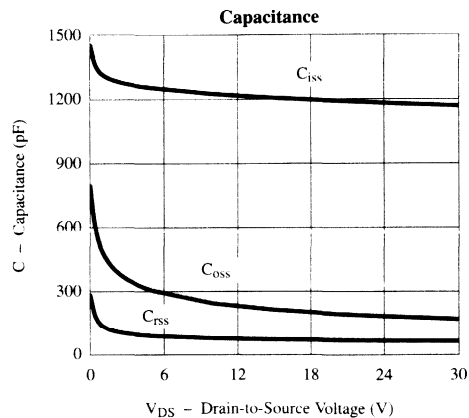
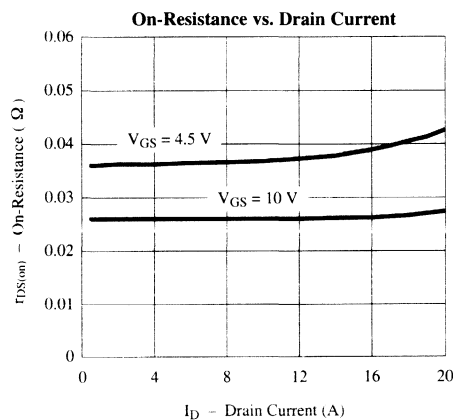
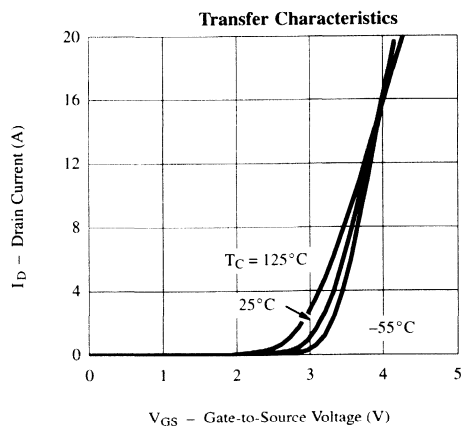
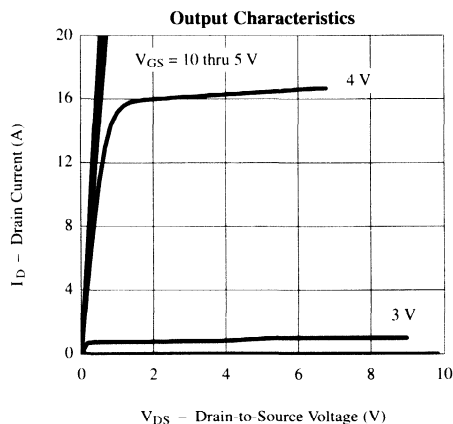
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 4.0\ \text{A}$		0.027	0.035	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 3.4\ \text{A}$		0.038	0.050	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 4.0\ \text{A}$		13		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.73	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 4.0\ \text{A}$		17.5	30	nC
Gate-Source Charge	Q_{gs}			4.0		
Gate-Drain Charge	Q_{gd}			2.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 6\ \Omega$ $I_D \approx 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		12	20	ns
Rise Time	t_r			9	20	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			20	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		25	60	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

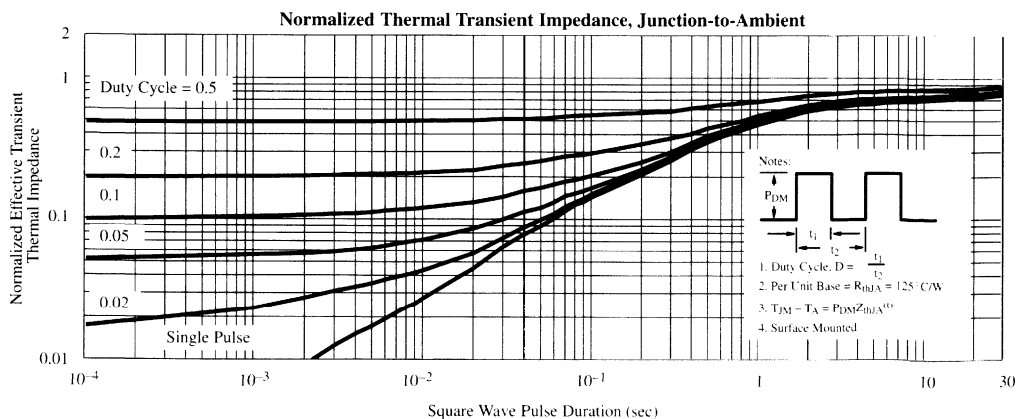
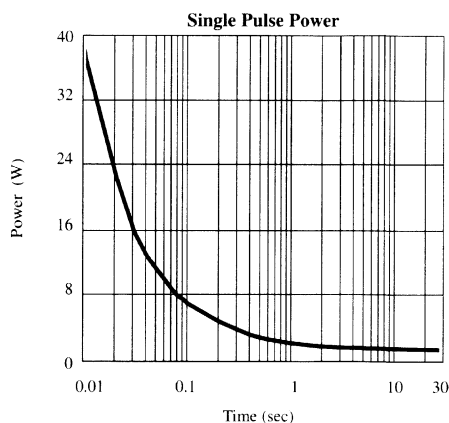
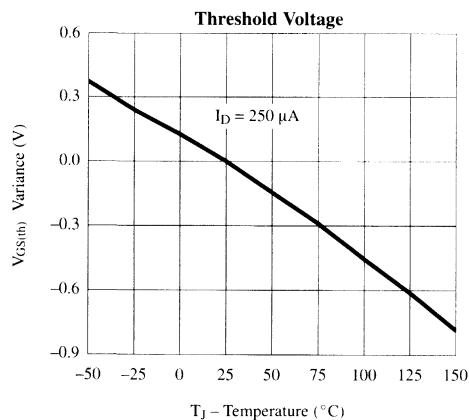
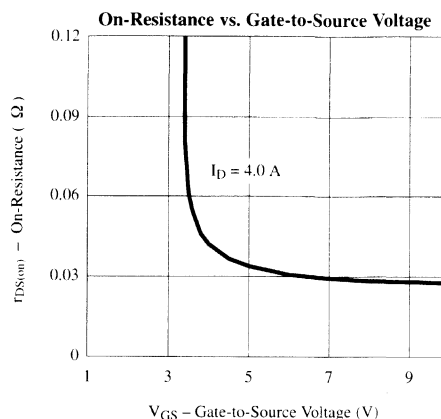
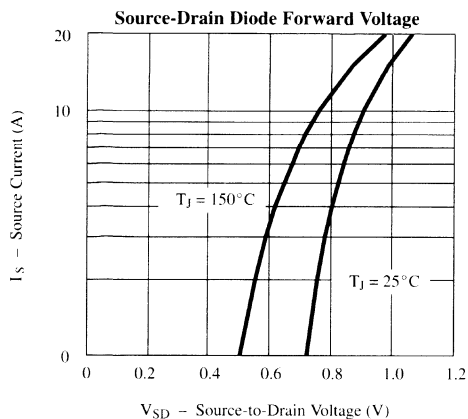
Typical Characteristics (25°C Unless Otherwise Noted)



2

TSSOP-8

Typical Characteristics (25°C Unless Otherwise Noted)

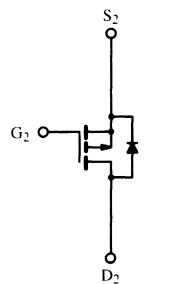
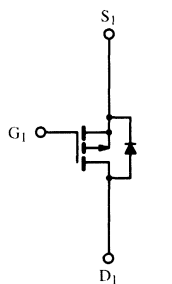
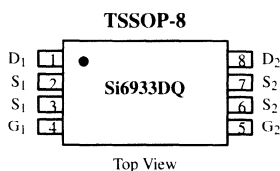


Dual P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-30	0.045 @ V _{GS} = -10 V	± 3.5
	0.085 @ V _{GS} = -4.5 V	± 2.5

TrenchFET™
Power MOSFETs



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 3.5	A
		± 2.8	
Pulsed Drain Current	I _{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I _S	-1.25	
Maximum Power Dissipation ^a	P _D	1.0	W
		0.64	
Operating Junction and Storage Temperature Range	T _J , T _{Stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70640.

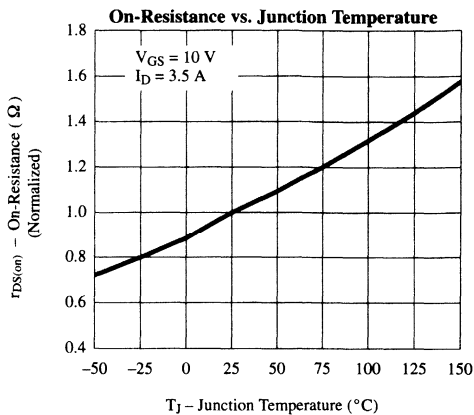
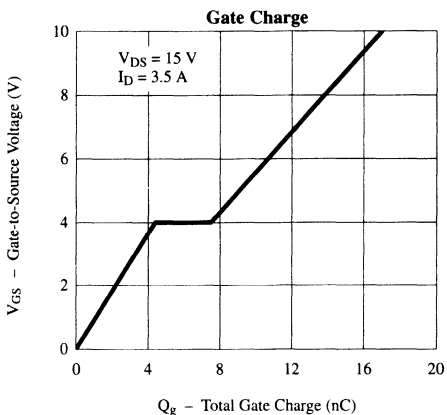
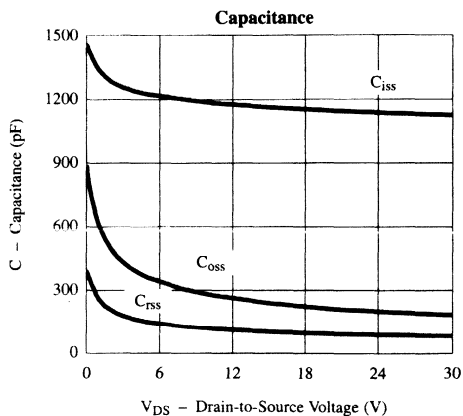
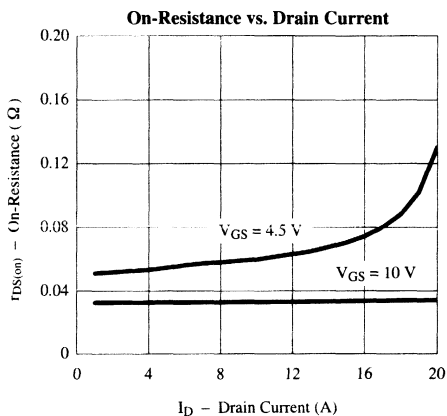
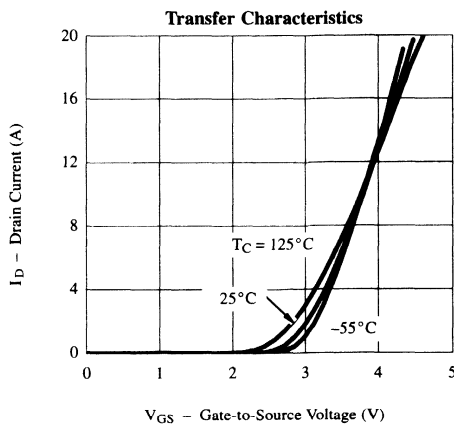
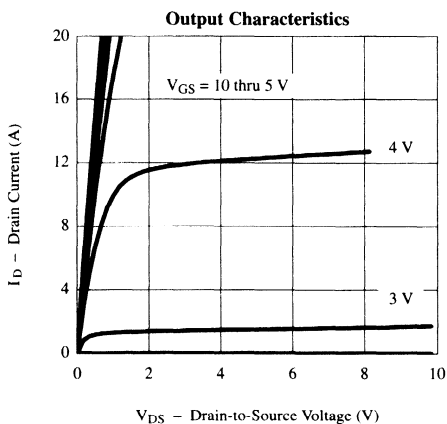
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\ \text{V}, V_{GS} = -10\ \text{V}$	-15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = 3.5\ \text{A}$		0.035	0.045	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = 2.5\ \text{A}$		0.062	0.085	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -3.5\ \text{A}$		7.2		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.25\ \text{A}, V_{GS} = 0\ \text{V}$		-0.77	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -3.5\ \text{A}$		17	30	nC
Gate-Source Charge	Q_{gs}			4.4		
Gate-Drain Charge	Q_{gd}			3.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong -I_A, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		13	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			33	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}			30	60	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

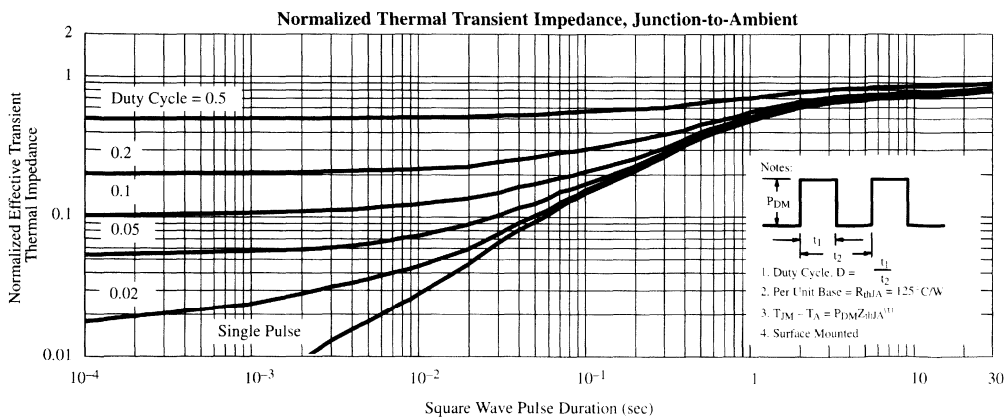
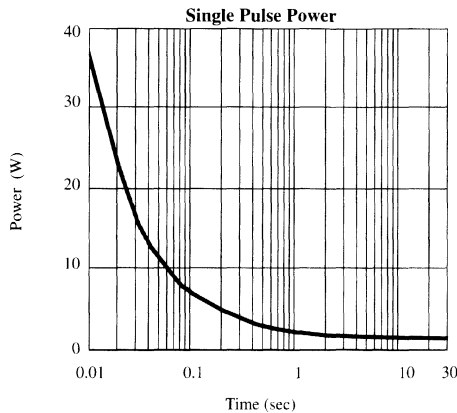
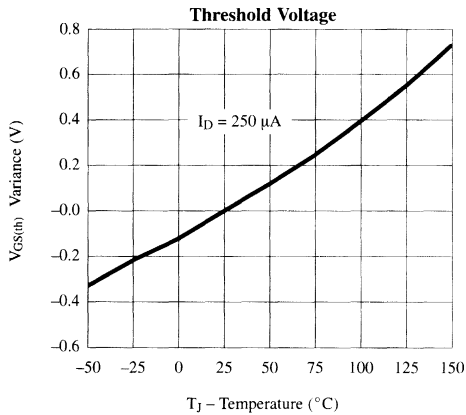
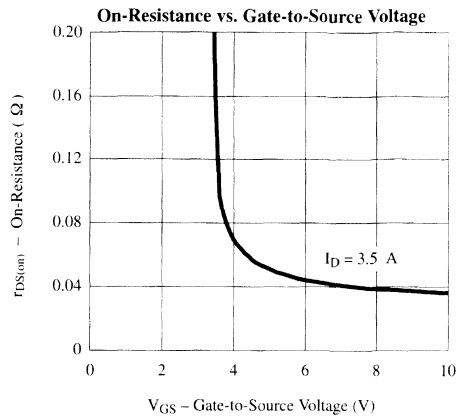
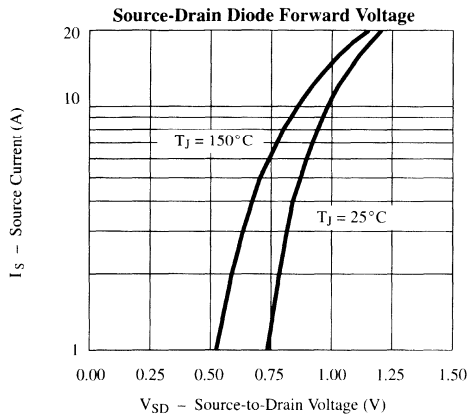
Typical Characteristics (25°C Unless Noted)



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TSSOP-8

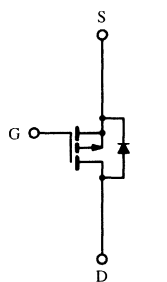
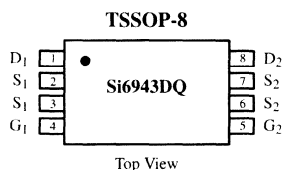
Typical Characteristics (25°C Unless Noted)



Dual P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.10 @ $V_{GS} = -4.5$ V	± 2.5
	0.18 @ $V_{GS} = -2.5$ V	± 1.9



2

TSSOP-8

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 2.5	A
		± 2.0	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	± 1	
Maximum Power Dissipation ^a	P_D	1.0	W
		0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70176. A SPICE Model data sheet is available for this product (FaxBack document #70548).

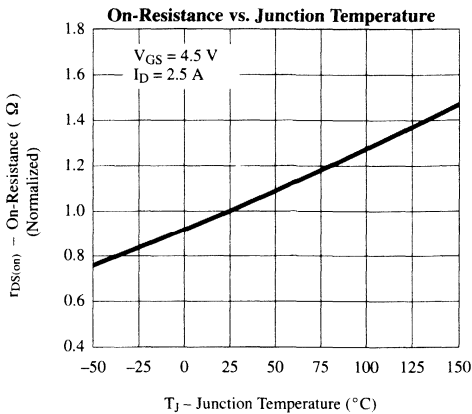
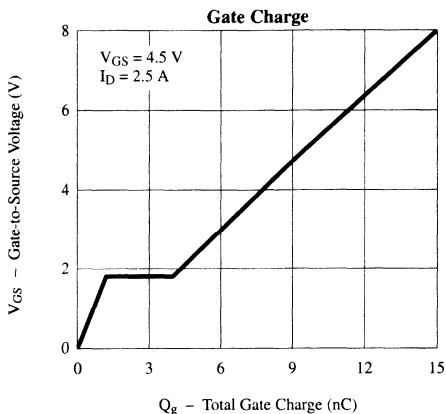
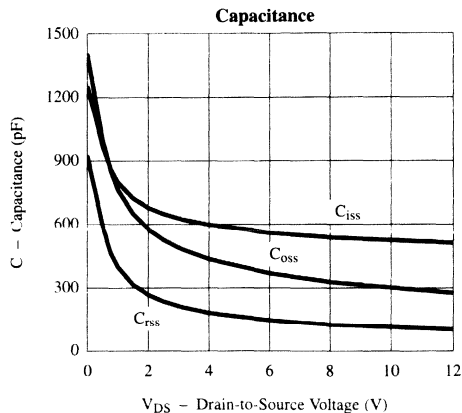
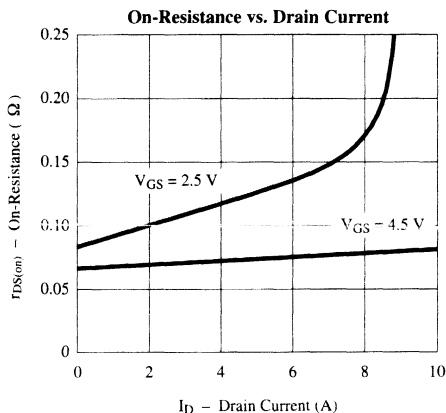
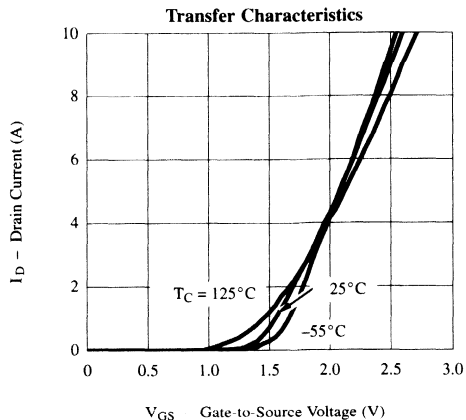
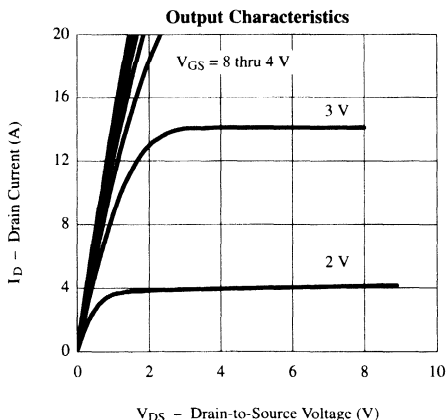
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -12\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-10			A
		$V_{DS} = -5\ \text{V}, V_{GS} = -2.5\ \text{V}$	-4			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = 2.5\ \text{A}$			0.10	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = 1.9\ \text{A}$			0.18	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -9\ \text{V}, I_D = -2.5\ \text{A}$		7		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.0\ \text{A}, V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -2.5\ \text{A}$		9	20	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\ \text{V}, R_L = 6\ \Omega$ $I_D \approx -1.0\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		21	40	ns
Rise Time	t_r			35	70	
Turn-Off Delay Time	$t_{d(off)}$			43	80	
Fall Time	t_f			22	40	
Source-Drain Reverse Recovery Time	t_{rr}			35	70	

Notes

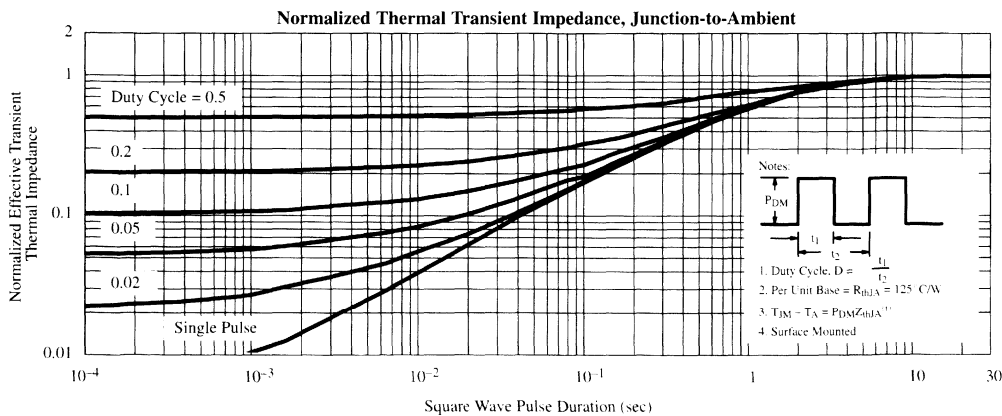
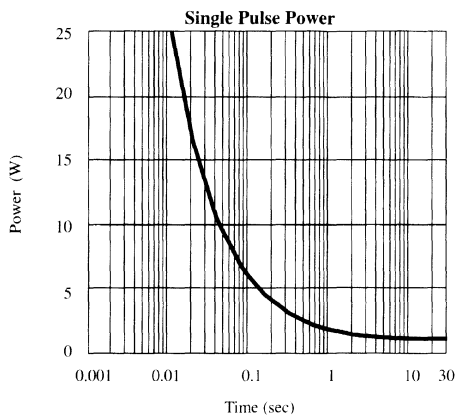
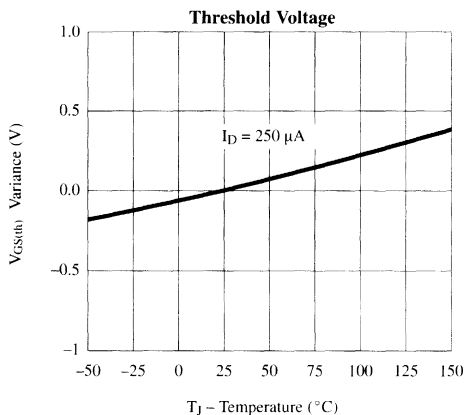
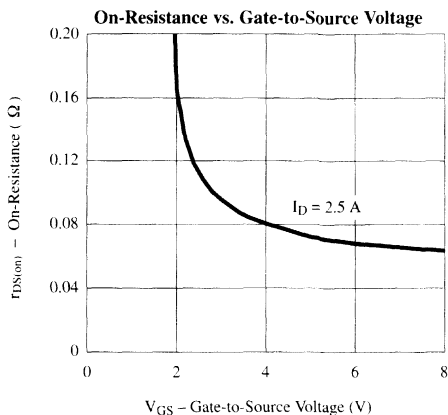
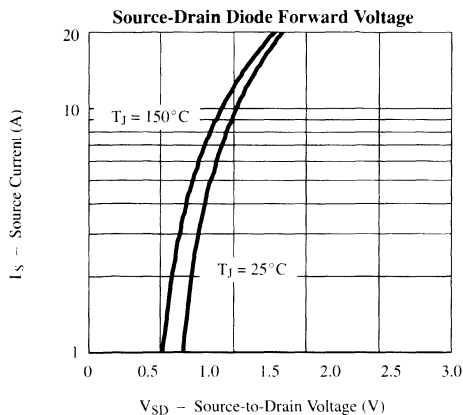
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



2

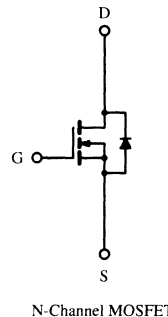
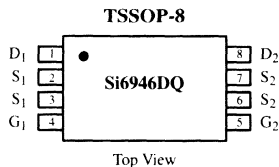
TSSOP-8

Typical Characteristics (25°C Unless Otherwise Noted)


Dual N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.080 @ $V_{GS} = 4.5$ V	2.8
	0.110 @ $V_{GS} = 2.5$ V	2.1



2
TSSOP-8

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	20	
Continuous Source Current (Diode Conduction) ^a	I_S	1.0	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70177. A SPICE Model data sheet is available for this product (FaxBack document #70549).

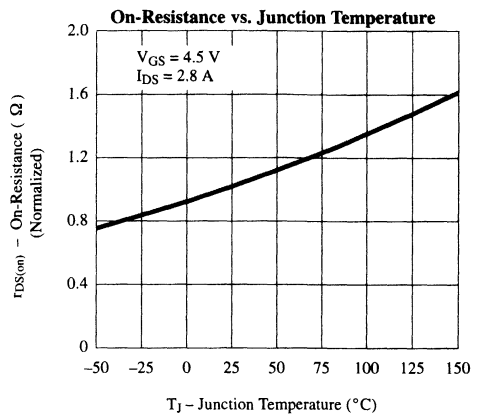
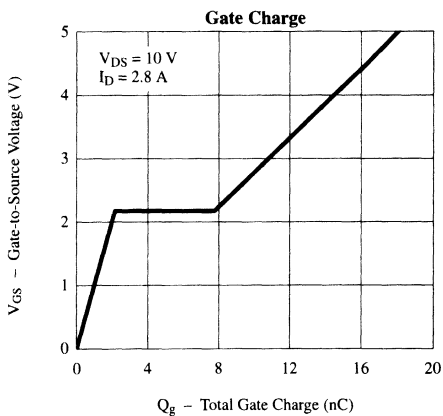
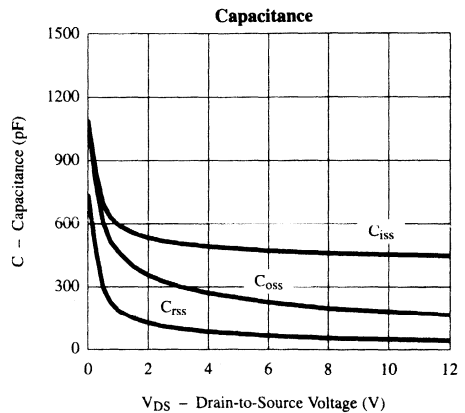
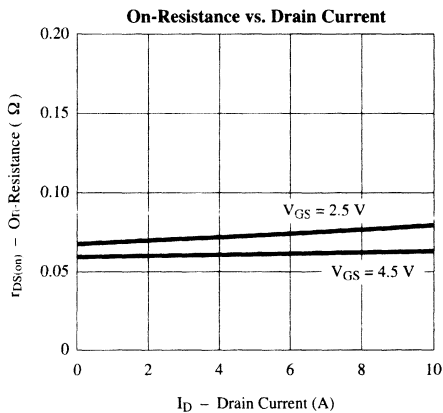
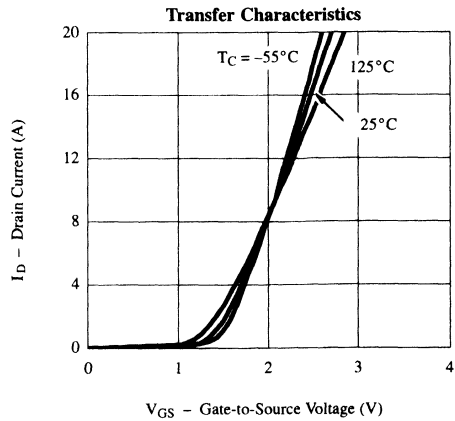
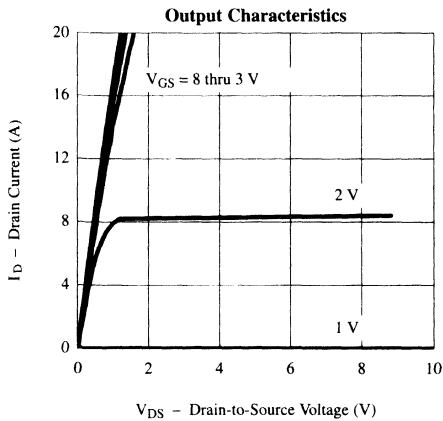
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	± 10			A
		$V_{DS} = 5\ \text{V}, V_{GS} = 2.5\ \text{V}$	± 4			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 2.8\ \text{A}$			0.080	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 2.1\ \text{A}$			0.110	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 2.8\ \text{A}$		12		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.0\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 2.8\ \text{A}$		16	40	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		37	60	ns
Rise Time	t_r			66	100	
Turn-Off Delay Time	$t_{d(off)}$			56	100	
Fall Time	t_f			57	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.0\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		26	70	

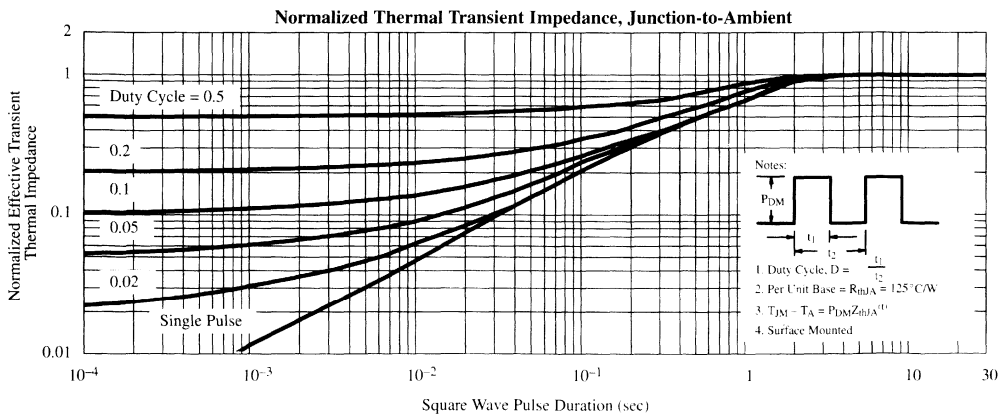
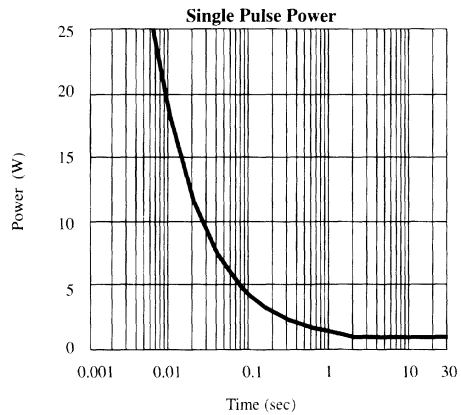
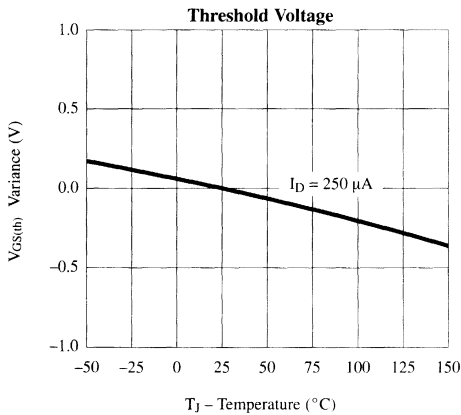
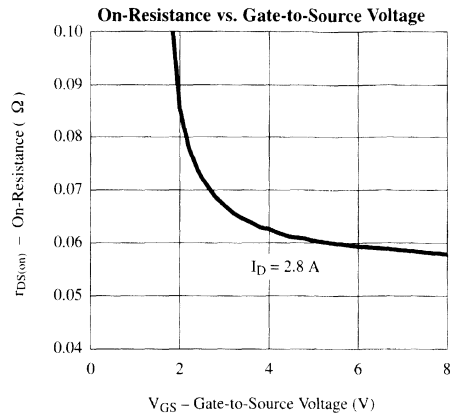
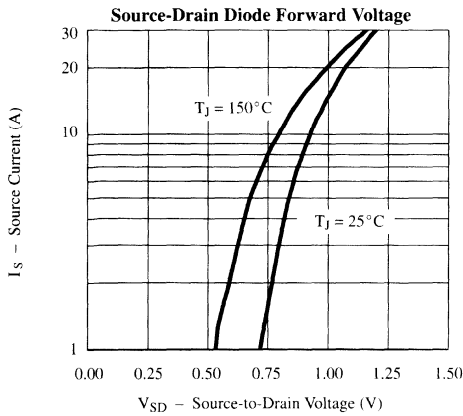
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



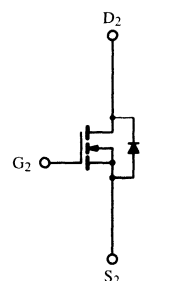
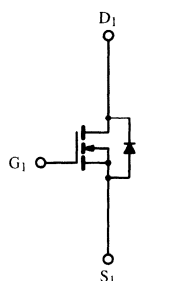
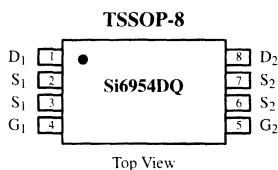
Typical Characteristics (25°C Unless Otherwise Noted)



Dual N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.065 @ $V_{GS} = 10$ V	± 3.9
	0.095 @ $V_{GS} = 4.5$ V	± 3.1



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 3.9	A
	$T_A = 70^\circ\text{C}$		± 3.1	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a		I_S	1.25	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.0	W
	$T_A = 70^\circ\text{C}$		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70179.

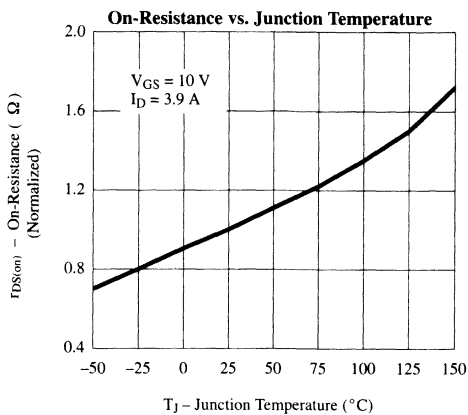
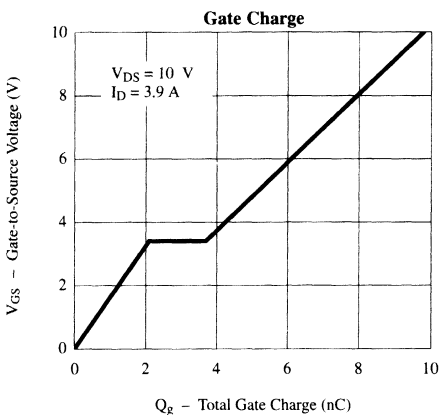
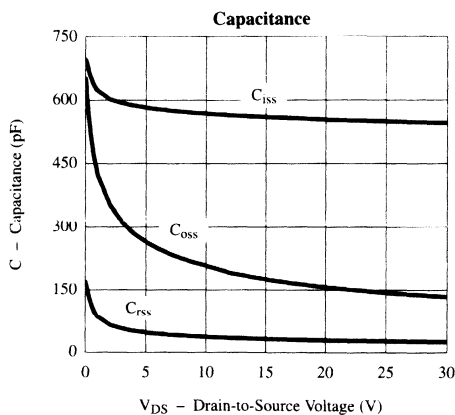
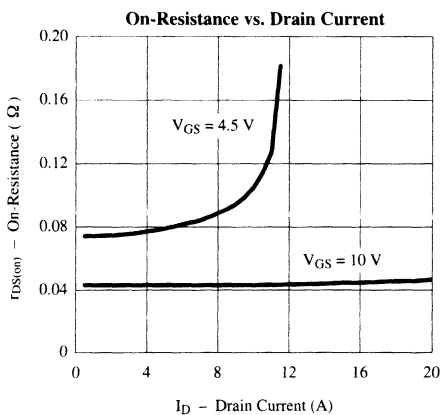
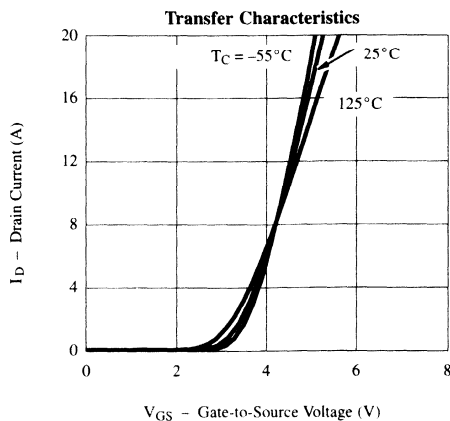
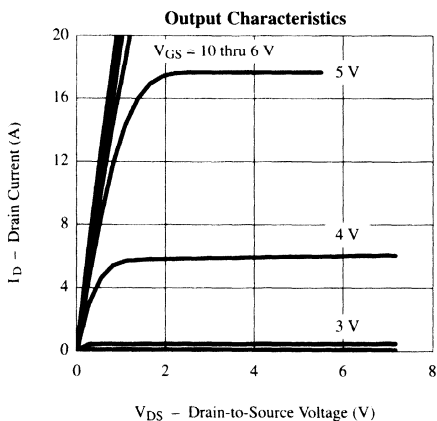
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 3.9\ \text{A}$		0.043	0.065	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 3.1\ \text{A}$		0.075	0.095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 3.9\ \text{A}$		7.0		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ \text{A}, V_{GS} = 0\ \text{V}$		0.77	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 3.9\ \text{A}$		9.8	15	nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		9	15	ns
Rise Time	t_r			6	12	
Turn-Off Delay Time	$t_{d(off)}$			18	27	
Fall Time	t_f			6	12	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		48	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

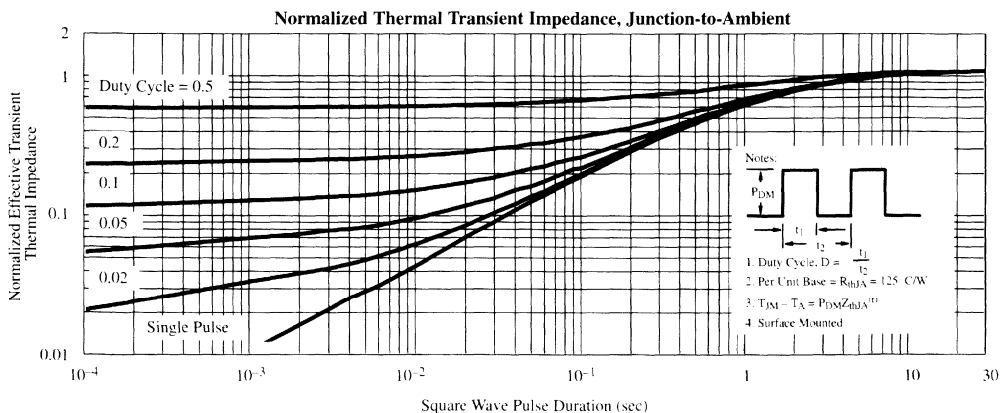
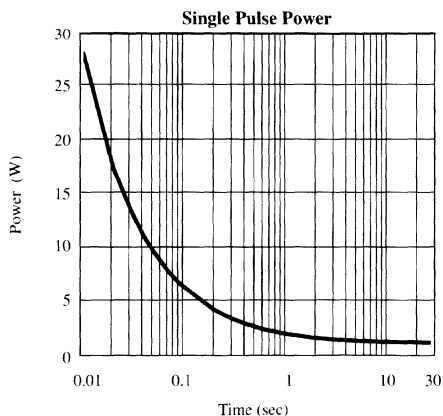
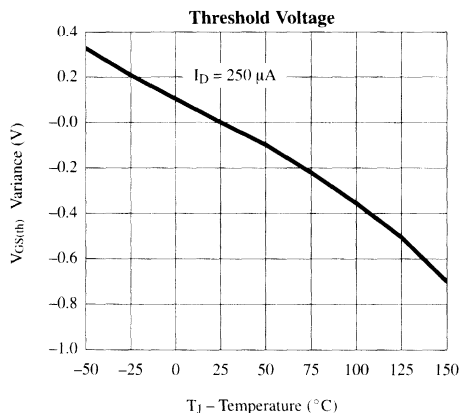
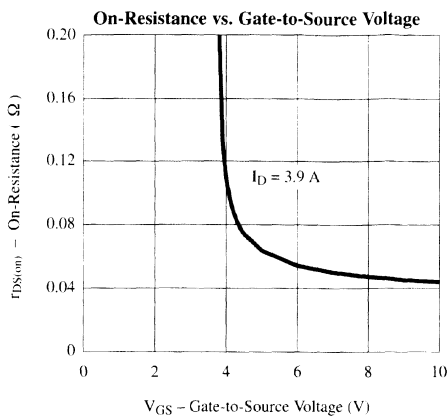
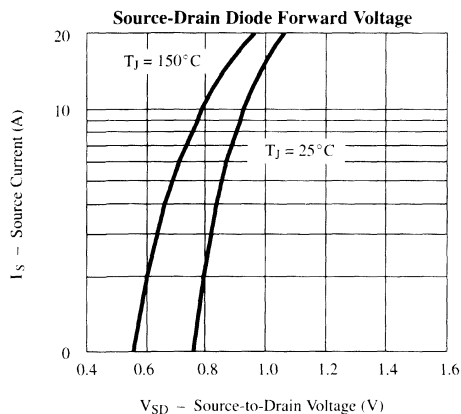
Typical Characteristics (25°C Unless Otherwise Noted)



2

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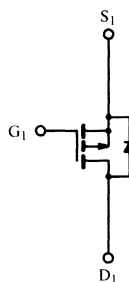
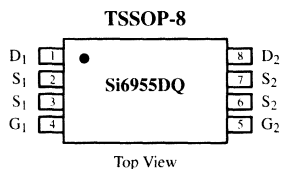
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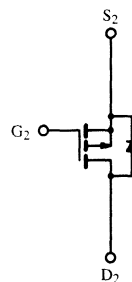
Dual P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.085 @ $V_{GS} = -10$ V	± 2.5
	0.19 @ $V_{GS} = -4.5$ V	± 1.8



P-Channel MOSFET



P-Channel MOSFET

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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 2.5	A
		± 2.1	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.25	
Maximum Power Dissipation ^a	P_D	1.0	W
		0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70180. A SPICE Model data sheet is available for this product (FaxBack document #70550).

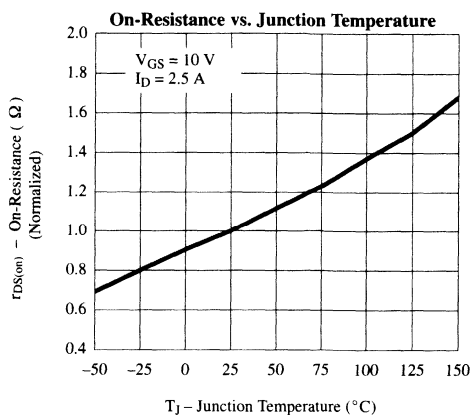
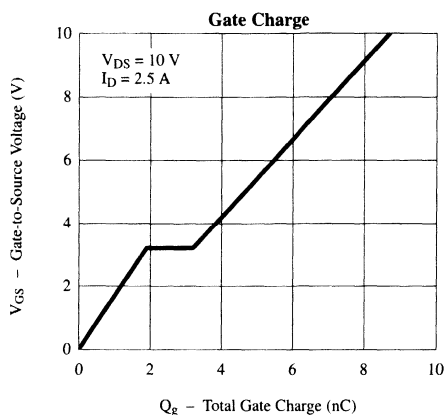
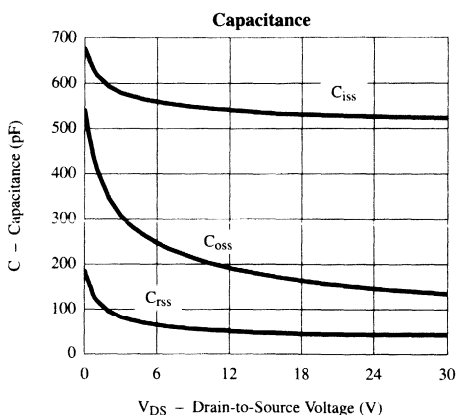
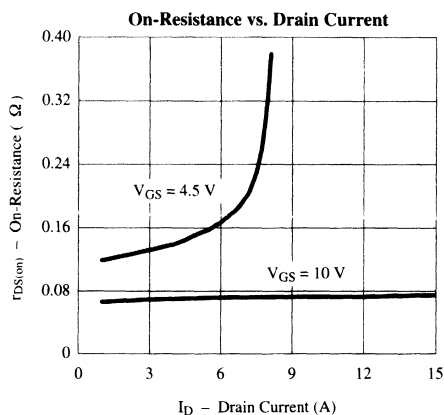
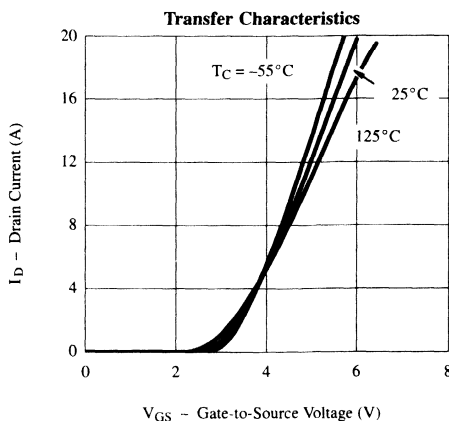
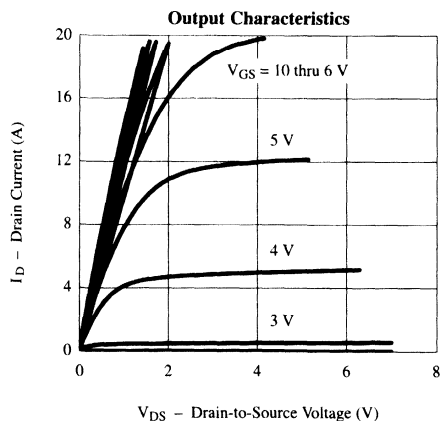
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\ \text{V}, V_{GS} = -10\ \text{V}$	-15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = 2.5\ \text{A}$		0.066	0.085	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = 1.8\ \text{A}$		0.125	0.19	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -2.5\ \text{A}$		5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.25\ \text{A}, V_{GS} = 0\ \text{V}$		0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -2.5\ \text{A}$		8.7	15	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		7	15	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			14	27	
Fall Time	t_f			8	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		46	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

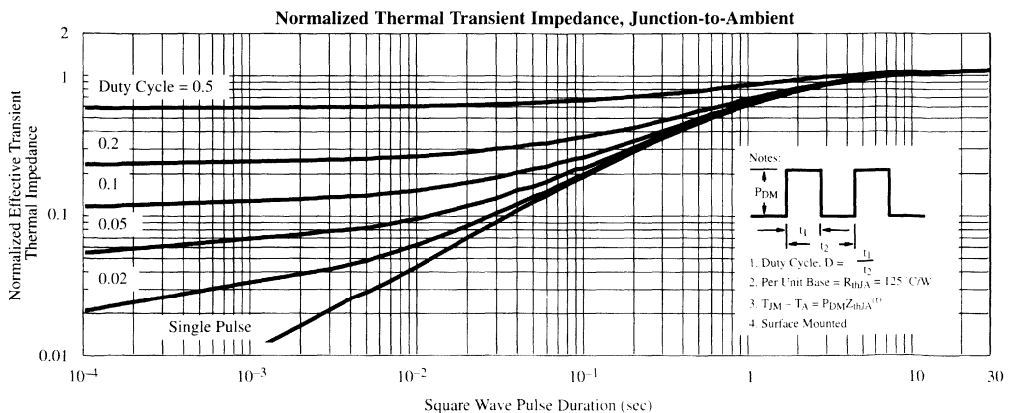
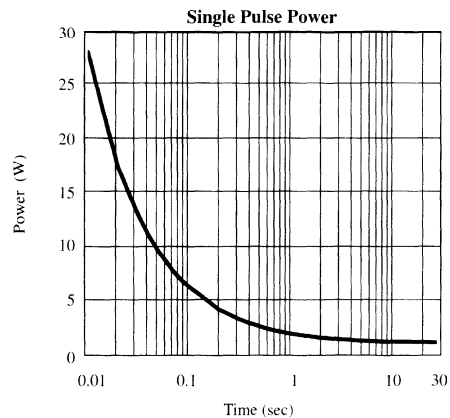
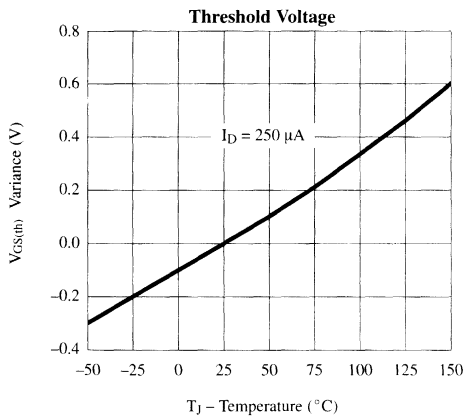
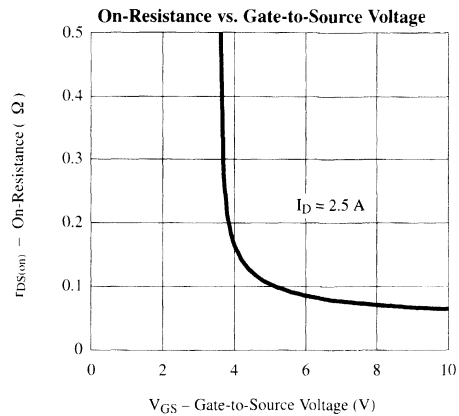
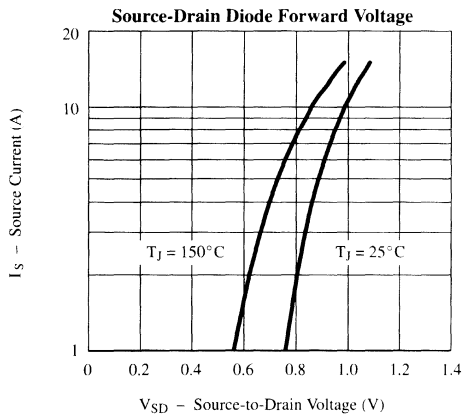
Typical Characteristics (25°C Unless Otherwise Noted)



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TSSOP-8

Typical Characteristics (25°C Unless Otherwise Noted)

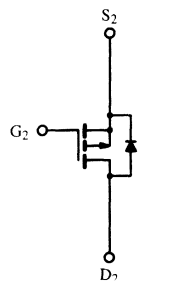
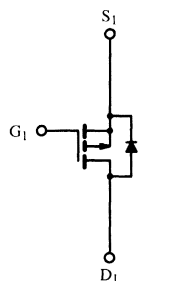
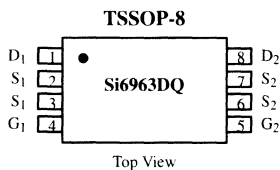


Dual P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-20	0.050 @ V _{GS} = -4.5 V	± 3.5
	0.085 @ V _{GS} = -2.5 V	± 2.7

TrenchFET™
Power MOSFETs
2.5-V Rated



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TSSOP-8

Absolute Maximum Ratings (T_A = 25 °C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	-20	V
Gate-Source Voltage		V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	± 3.5	A
	T _A = 70 °C		± 2.8	
Pulsed Drain Current		I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a		I _S	-1.25	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	1.0	W
	T _A = 70 °C		0.64	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70629.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

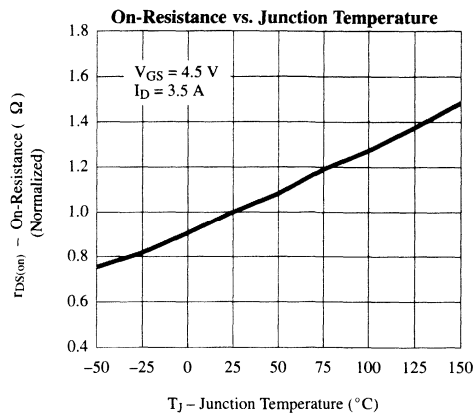
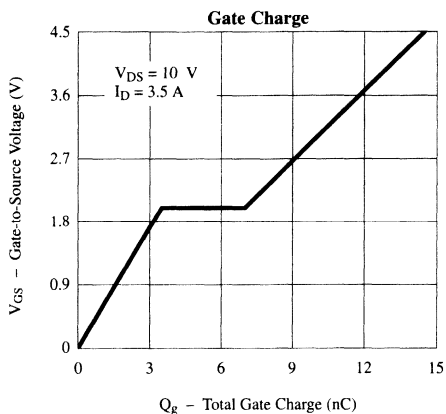
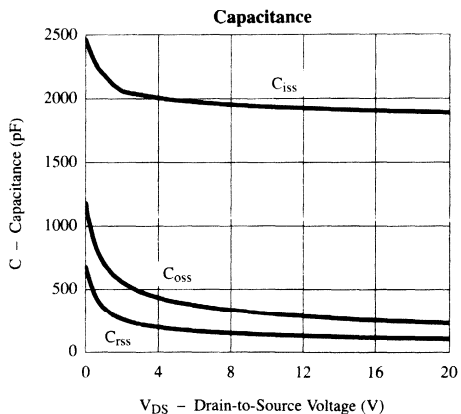
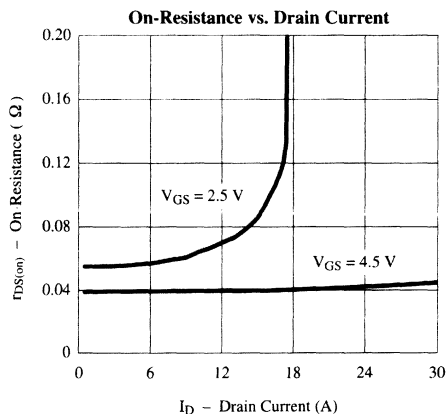
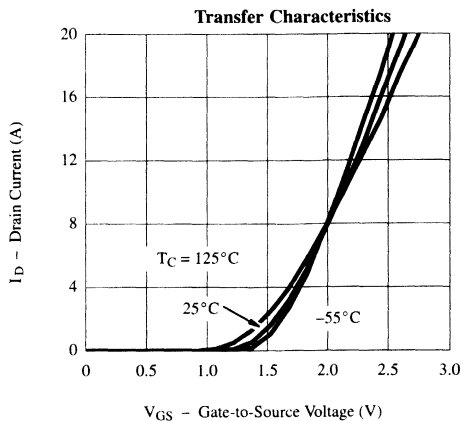
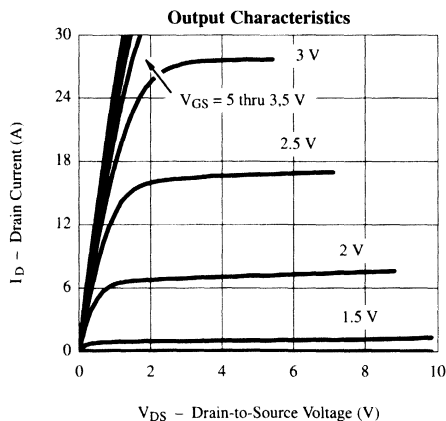
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -3.5\ \text{A}$		0.040	0.050	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -2.7\ \text{A}$		0.06	0.085	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -3.5\ \text{A}$		10		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.25\ \text{A}, V_{GS} = 0\ \text{V}$		-0.72	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -3.5\ \text{A}$		14.5	25	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		27	50	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			57	100	
Fall Time	t_f			21	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	100	

Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

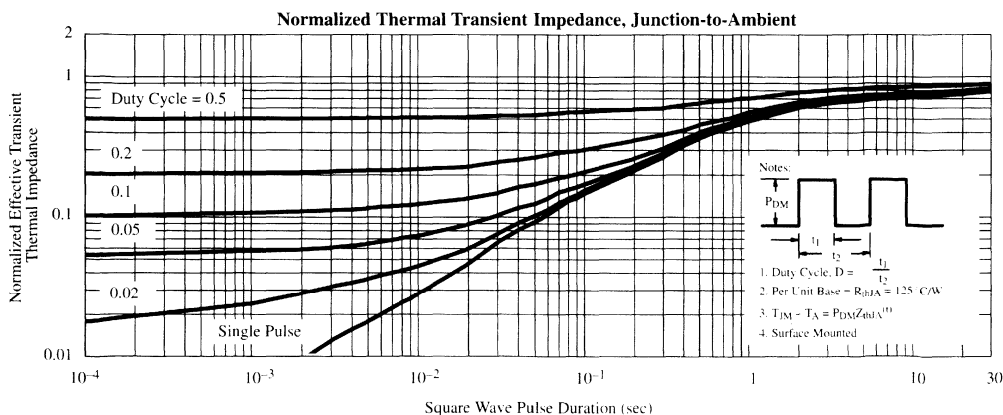
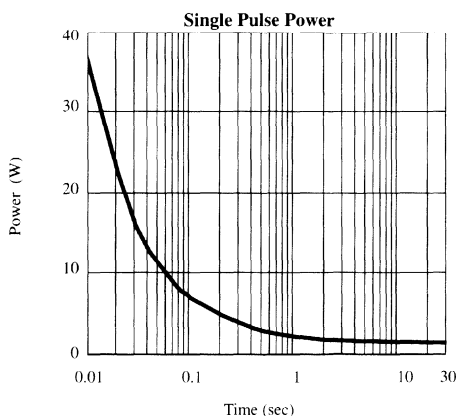
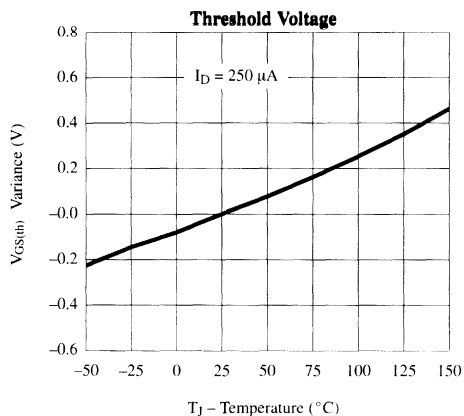
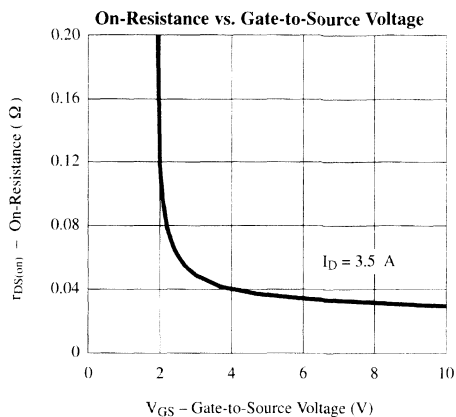
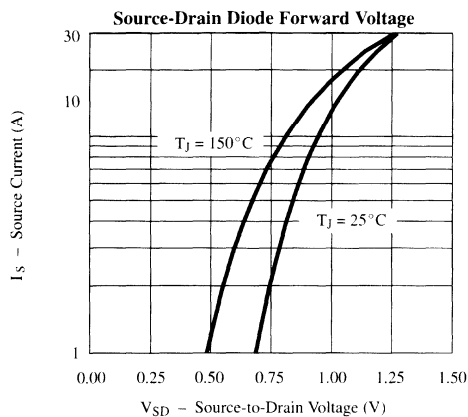
Typical Characteristics (25°C Unless Otherwise Noted)



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TSSOP-8

Typical Characteristics (25°C Unless Noted)

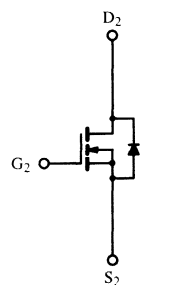
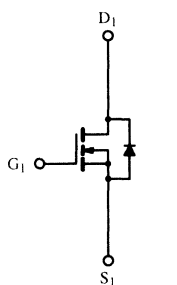
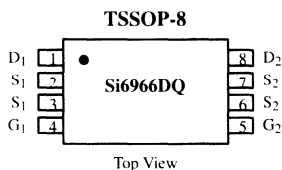


Dual N-Channel, 2.5-V (G-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.030 @ V _{GS} = 4.5 V	± 4.5
	0.040 @ V _{GS} = 2.5 V	± 3.9

TrenchFET™
Power MOSFETs
2.5-V Rated



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TSSOP-8

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 12	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 4.5	A
		± 3.6	
Pulsed Drain Current	I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I _S	1.25	W
Maximum Power Dissipation ^a	P _D	1.0	
		0.64	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70721.

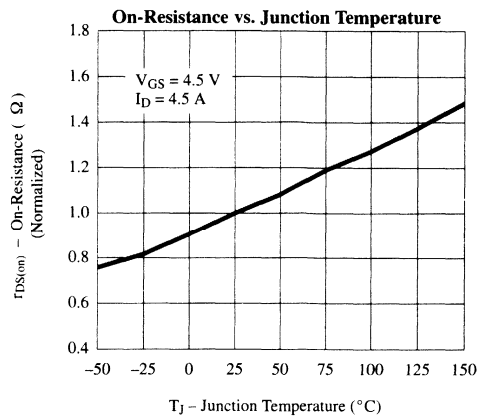
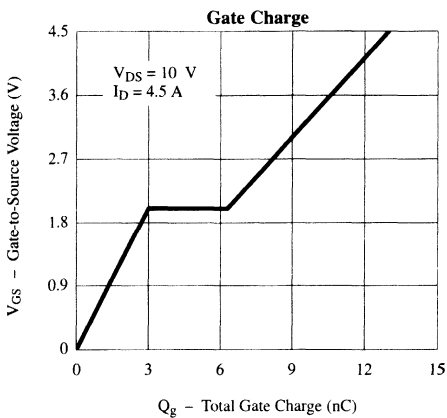
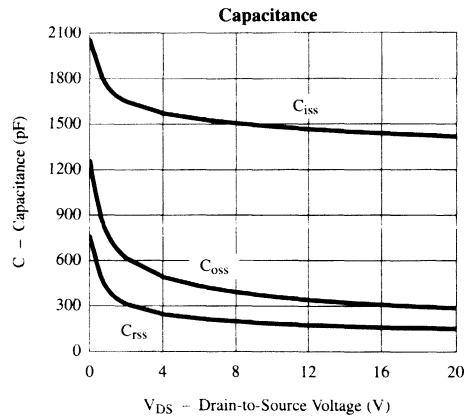
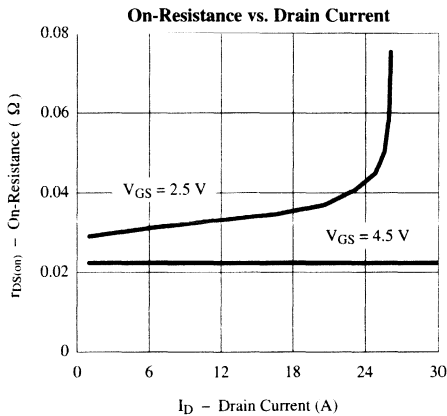
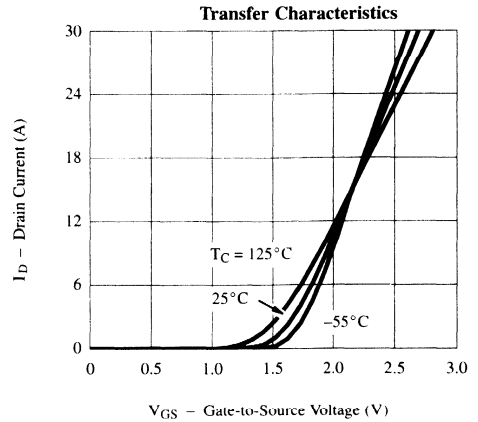
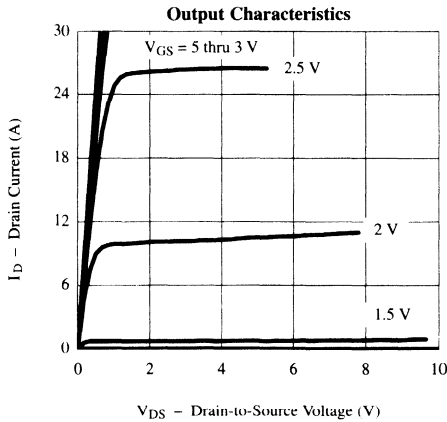
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 4.5\ \text{A}$		0.023	0.030	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 3.9\ \text{A}$		0.030	0.040	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 4.5\ \text{A}$		20		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\ \text{A}, V_{GS} = 0\ \text{V}$		0.65	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 4.5\ \text{A}$		13	25	nC
Gate-Source Charge	Q_{gs}			3.0		
Gate-Drain Charge	Q_{gd}			3.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		22	50	ns
Rise Time	t_r			40	80	
Turn-Off Delay Time	$t_{d(off)}$			50	100	
Fall Time	t_f			20	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		30	60	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

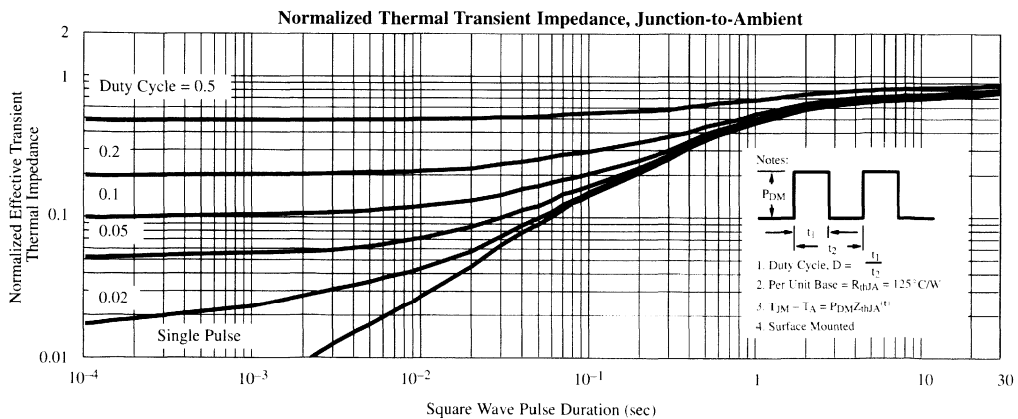
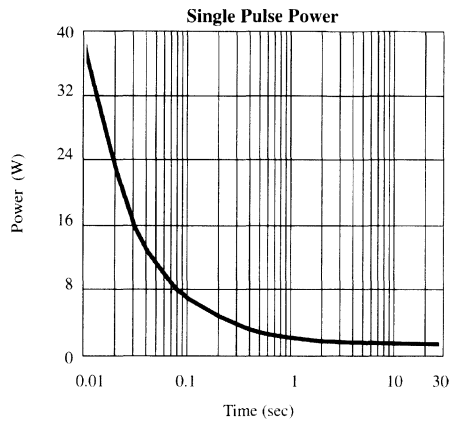
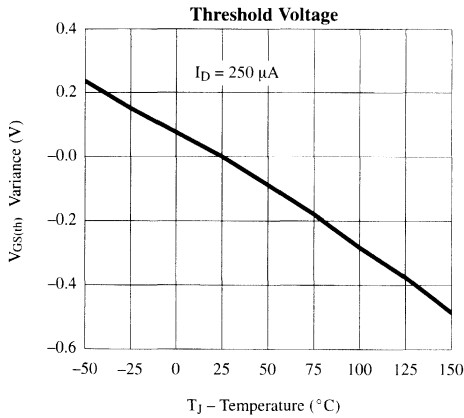
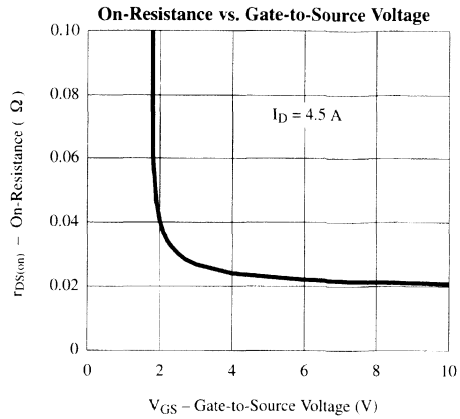
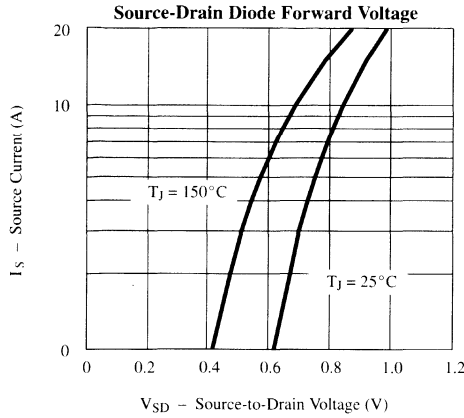
Typical Characteristics (25°C Unless Otherwise Noted)



2

TSSOP-8

Typical Characteristics (25°C Unless Otherwise Noted)

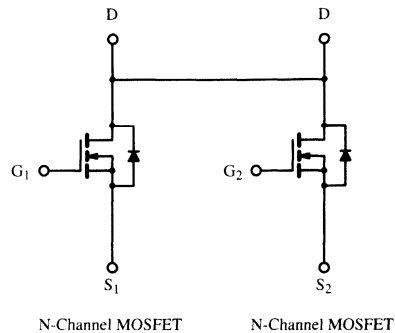
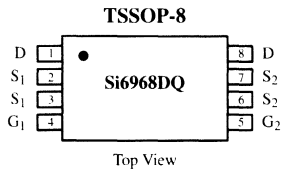


Dual N-Ch. 2.5-V (G-S) Rated MOSFET Common Drain

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.022 @ V _{GS} = 4.5 V	±6.5
	0.030 @ V _{GS} = 2.5 V	±5.5

2.5-V Rated



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±12	
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	A
		T _A = 70°C	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	±30	
Continuous Source Current (Diode Conduction) ^a	I _S	1.5	
Maximum Power Dissipation ^a	P _D	T _A = 25°C	W
		T _A = 70°C	
Operating Junction and Storage Temperature Range	T _J , T _{sig}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	83	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70757.

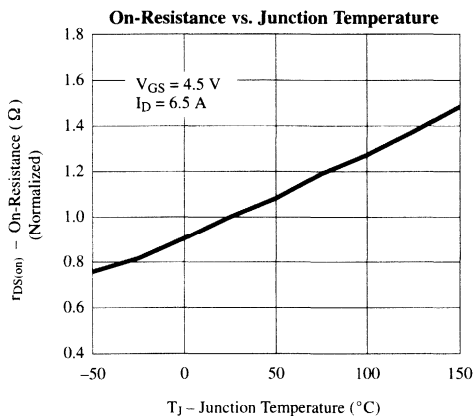
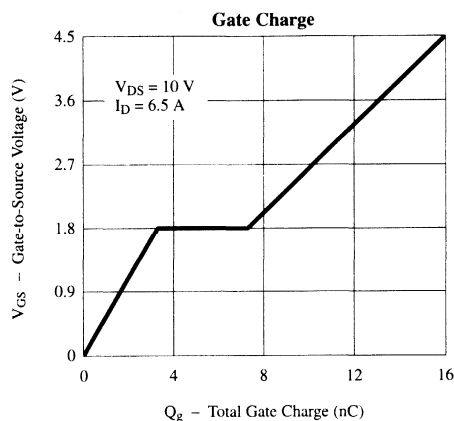
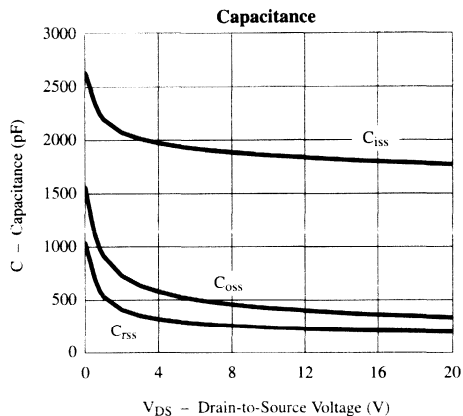
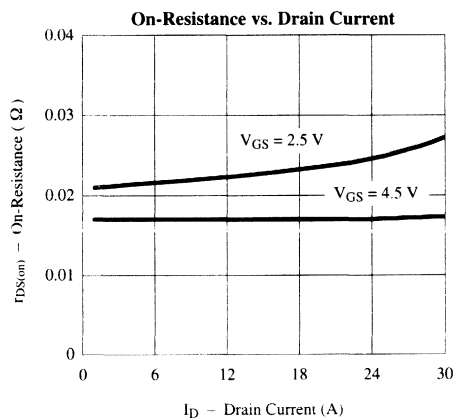
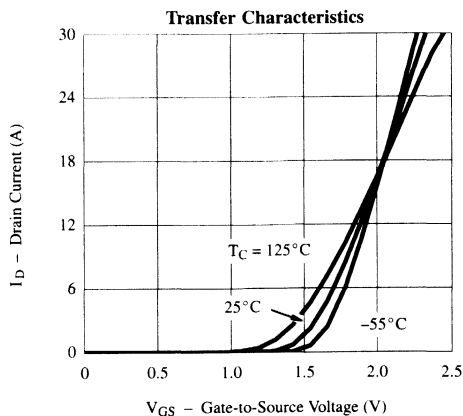
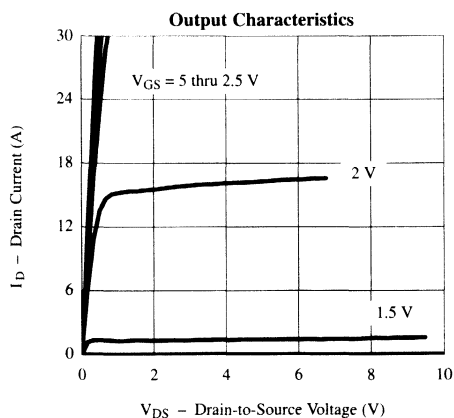
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 4.5\ \text{V}$	30			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}$, $I_D = 6.5\ \text{A}$		0.017	0.022	Ω
		$V_{GS} = 2.5\ \text{V}$, $I_D = 5.5\ \text{A}$		0.022	0.030	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 6.5\ \text{A}$		30		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.5\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.66	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 6.5\ \text{A}$		16	30	nC
Gate-Source Charge	Q_{gs}			3.4		
Gate-Drain Charge	Q_{gd}			4.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 4.5\ \text{V}$, $R_G = 6\ \Omega$		20	40	ns
Rise Time	t_r			48	80	
Turn-Off Delay Time	$t_{d(off)}$			90	180	
Fall Time	t_f			55	110	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.5\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		40	70	

Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

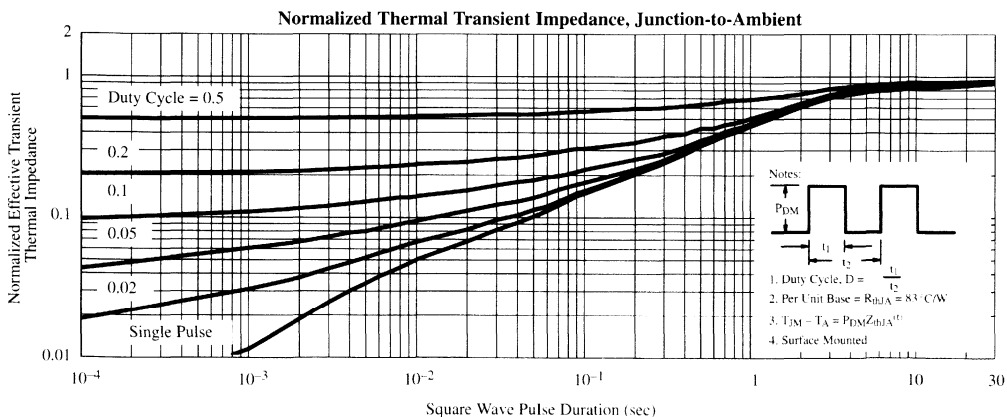
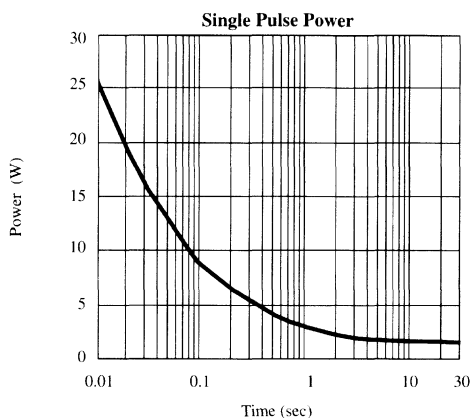
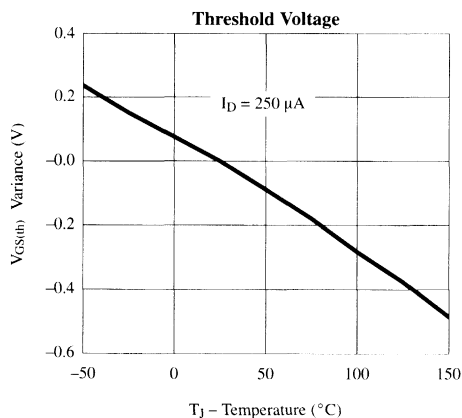
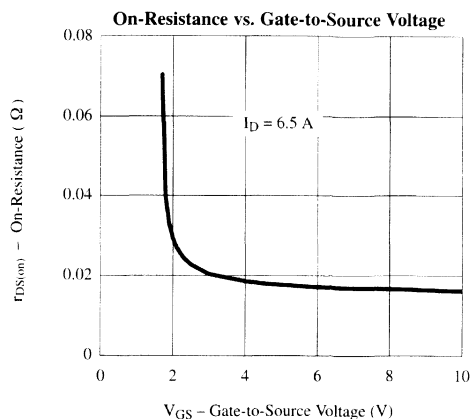
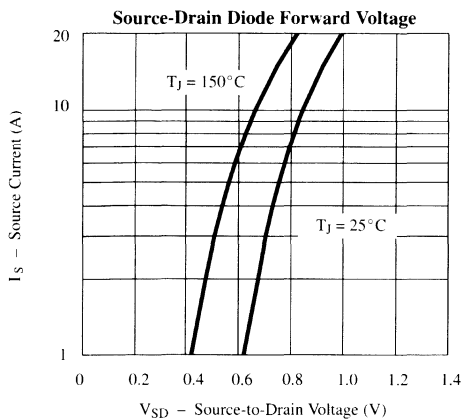
Typical Characteristics (25°C Unless Otherwise Noted)



2

TSSOP-8

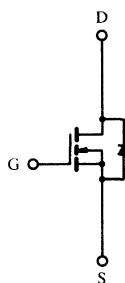
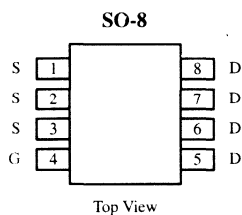
Typical Characteristics (25°C Unless Otherwise Noted)



N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0135 @ $V_{GS} = 10$ V	± 10
	0.020 @ $V_{GS} = 4.5$ V	± 8



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 10
	$T_A = 70^\circ\text{C}$		± 8
Pulsed Drain Current	I_{DM}	± 50	A
Continuous Source Current (Diode Conduction) ^a	I_S	2.3	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.5
	$T_A = 70^\circ\text{C}$		1.6
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70148. A SPICE Model data sheet is available for this product (FaxBack document #70534).

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

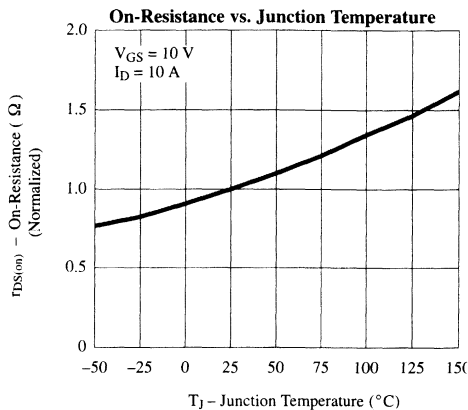
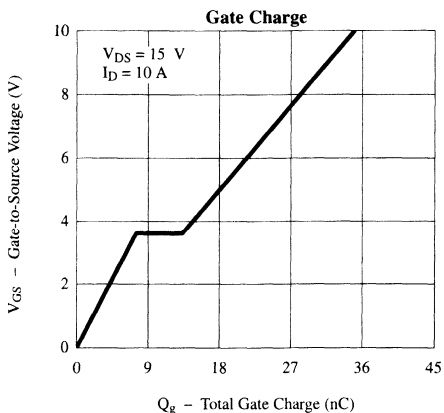
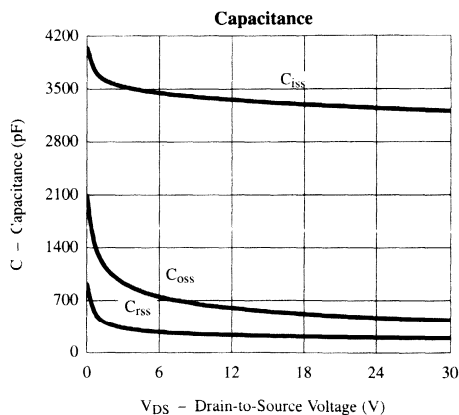
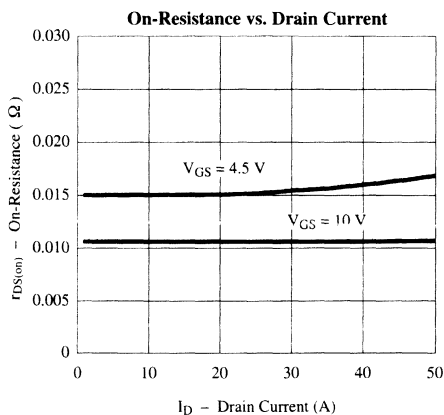
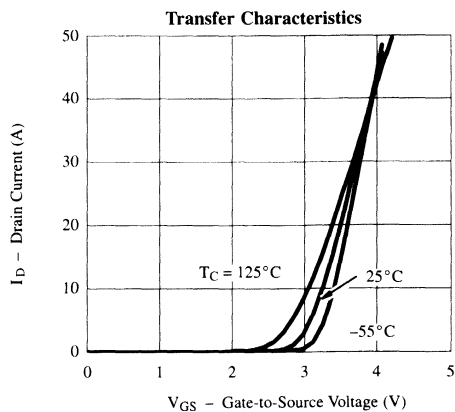
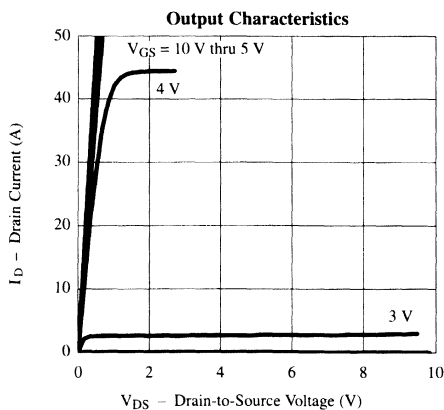
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 10\ \text{A}$		0.011	0.0135	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 5\ \text{A}$		0.015	0.020	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 10\ \text{A}$		38		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.3\ \text{A}, V_{GS} = 0\ \text{V}$		0.7	1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 10\ \text{A}$		35	60	nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			5.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25\ \text{V}, R_L = 25\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		15	30	ns
Rise Time	t_r			9	20	
Turn-Off Delay Time	$t_{d(off)}$			70	100	
Fall Time	t_f			20	80	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

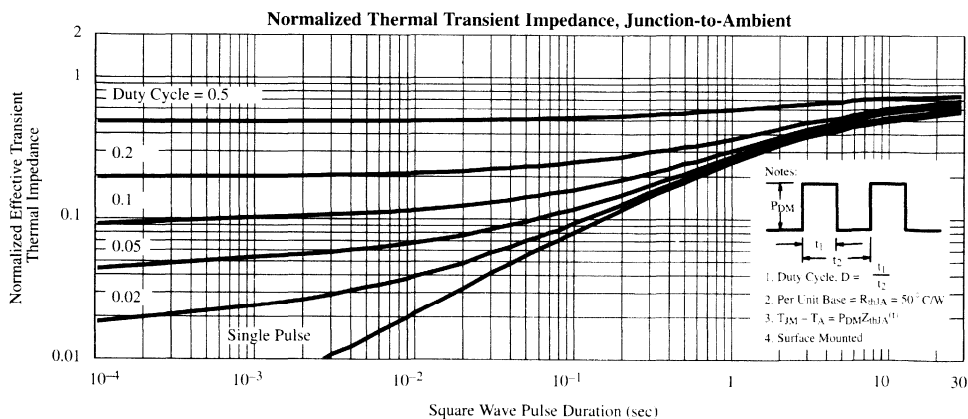
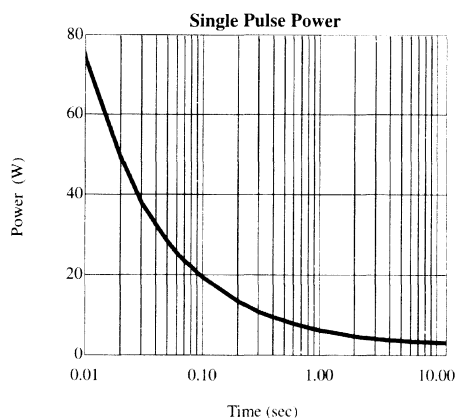
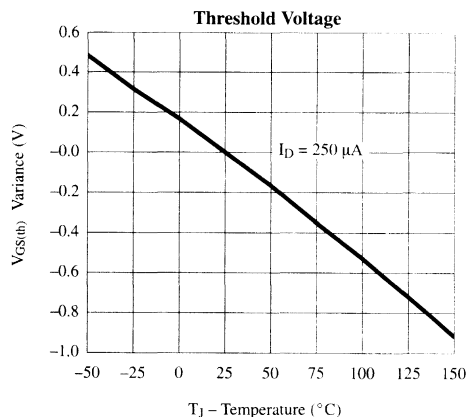
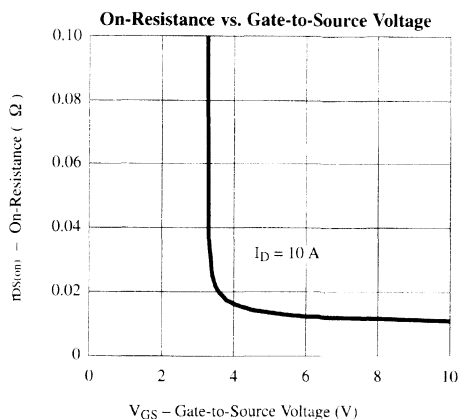
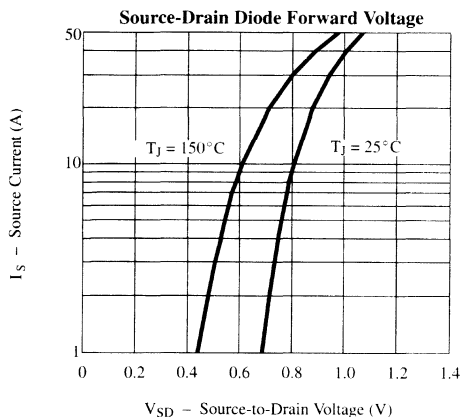
a. Guaranteed by design, not subject to production testing. Values shown are for product revision A.

 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics, Product Revision A (25°C Unless Noted)



Typical Characteristics, Product Revision A (25°C Unless Noted)

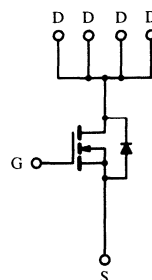
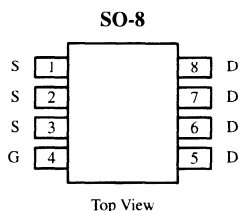


N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.018 @ $V_{GS} = 10$ V	± 9.0
	0.028 @ $V_{GS} = 4.5$ V	± 7.3

TrenchFET™
Power MOSFETs



N-Channel MOSFET

3

SOIC-8

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 9.0	A
		± 7.2	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	W
Maximum Power Dissipation ^a	P_D	2.5	
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70752.

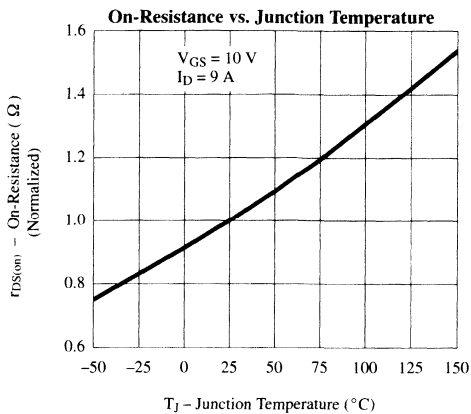
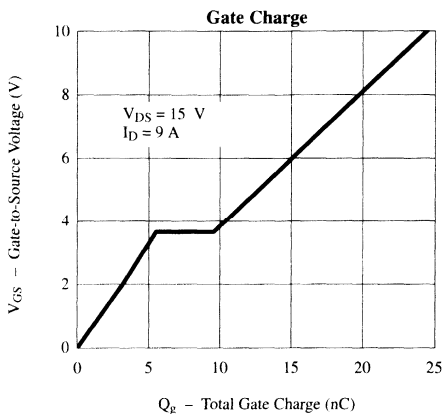
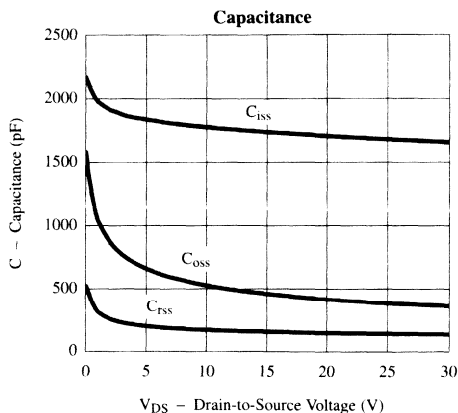
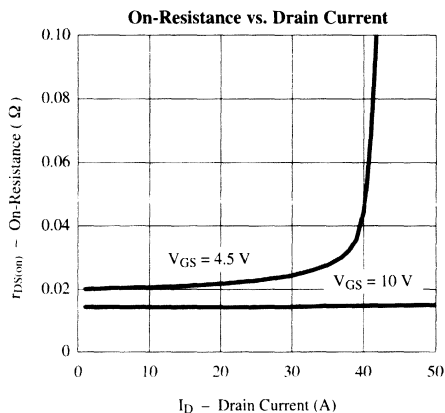
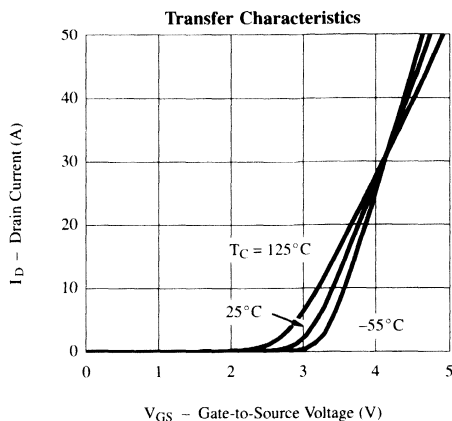
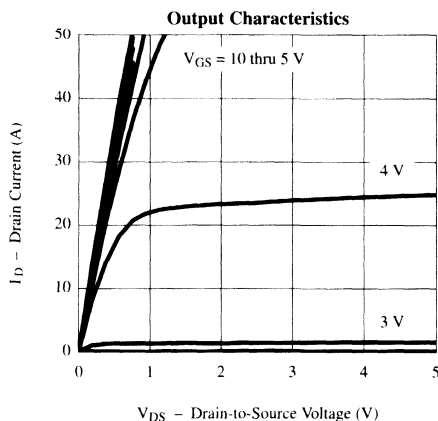
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

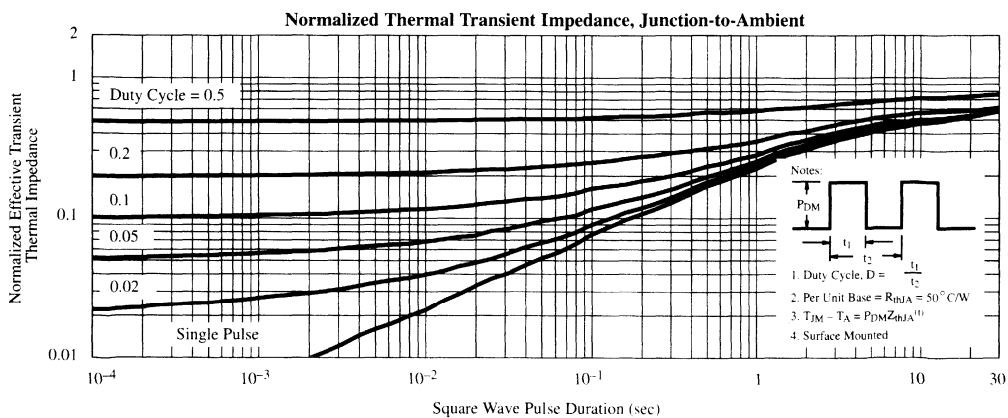
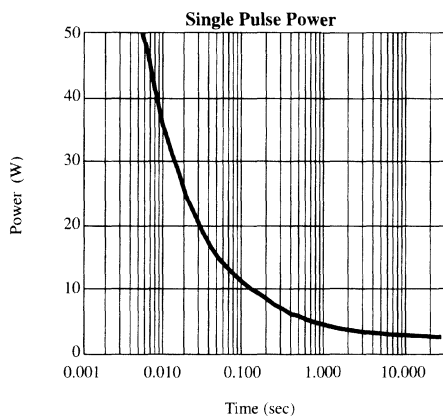
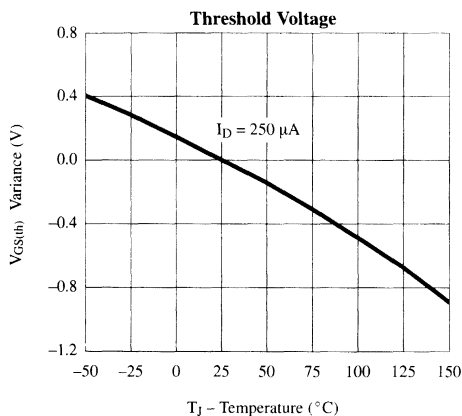
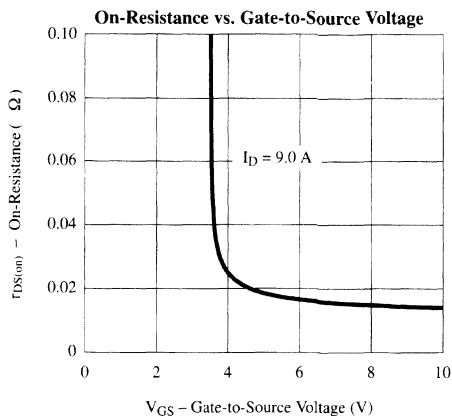
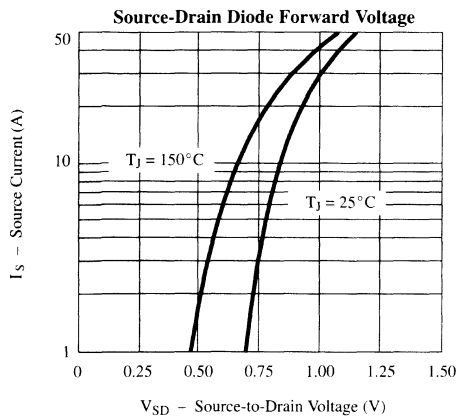
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 9.0\ \text{A}$		0.014	0.018	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 7.3\ \text{A}$		0.021	0.028	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 9.0\ \text{A}$		27		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.1\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 9.0\ \text{A}$		24	35	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D \equiv 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		12	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			32	50	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	90	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)



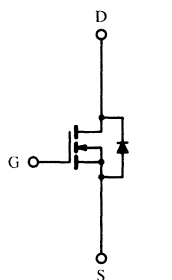
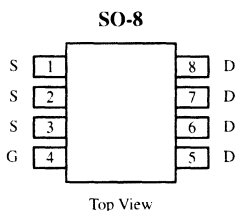
Typical Characteristics (25°C Unless Otherwise Noted)


N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.009 @ $V_{GS} = 10$ V	± 12.5
	0.013 @ $V_{GS} = 4.5$ V	± 10.5

TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 12.5	A
	$T_A = 70^\circ\text{C}$		± 10.0	
Pulsed Drain Current		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	2.3	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70647.

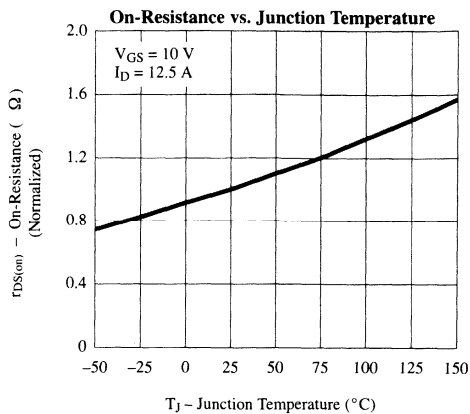
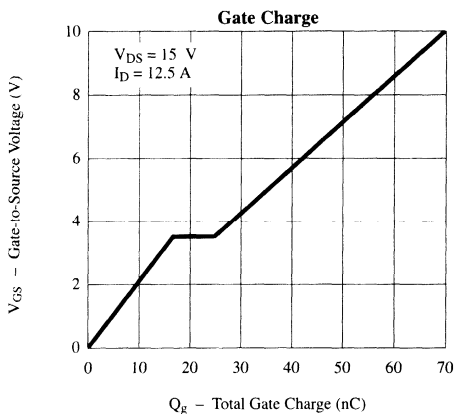
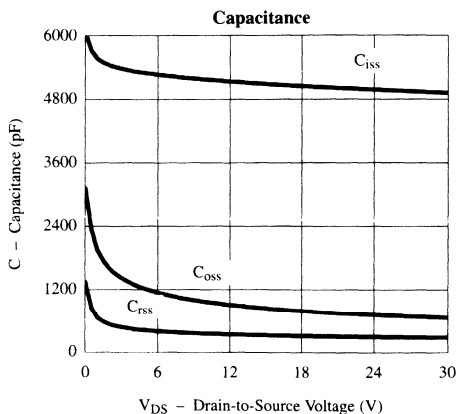
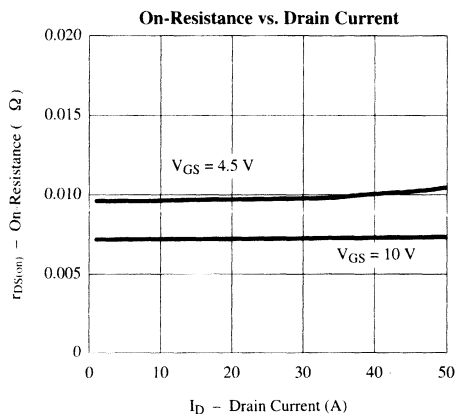
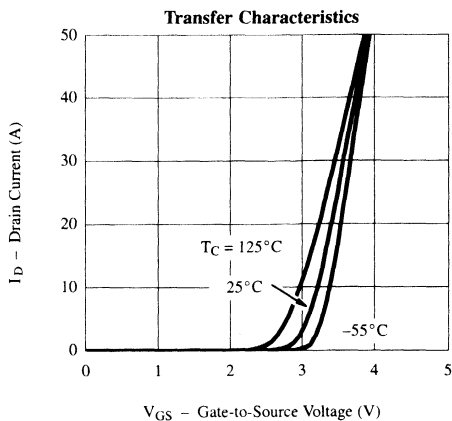
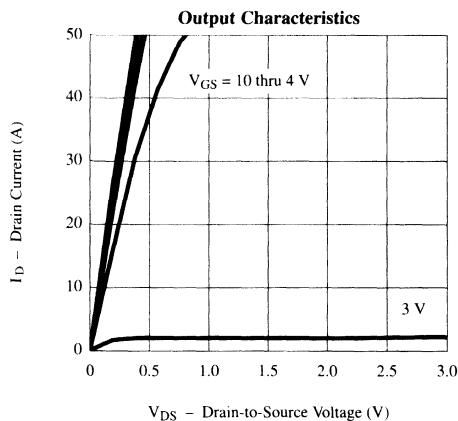
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 12.5\ \text{A}$		0.0075	0.009	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 10.5\ \text{A}$		0.010	0.013	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 12.5\ \text{A}$		50		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.3\ \text{A}$, $V_{GS} = 0\ \text{V}$			1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 12.5\ \text{A}$		70	120	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \approx 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		16	25	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			120	200	
Fall Time	t_f			35	70	
Source-Drain Reverse Recovery Time	t_{rr}			49	90	

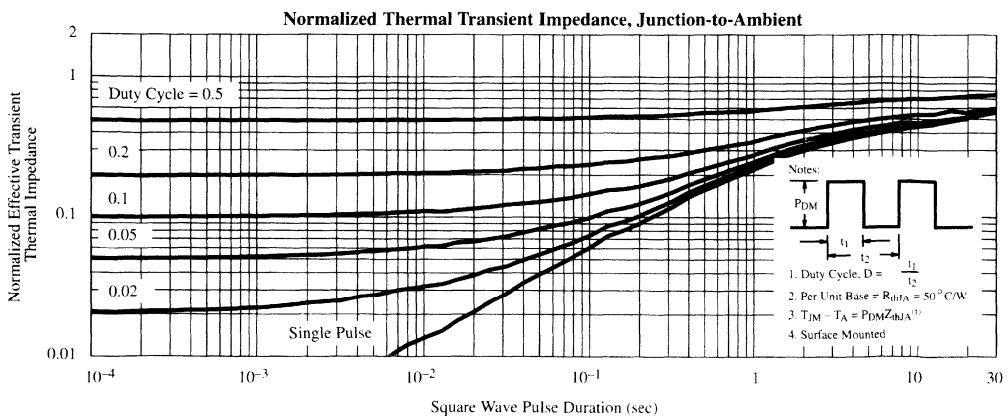
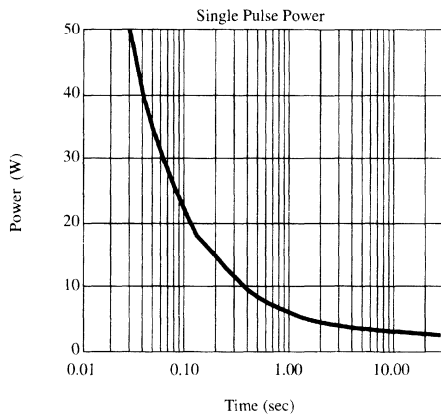
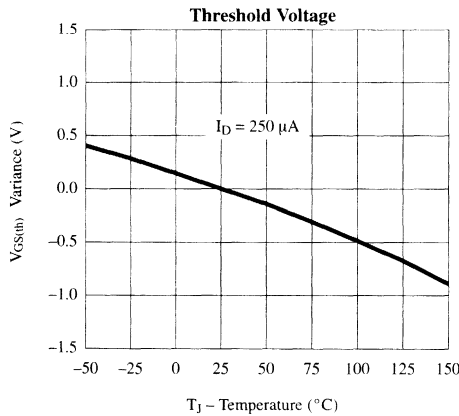
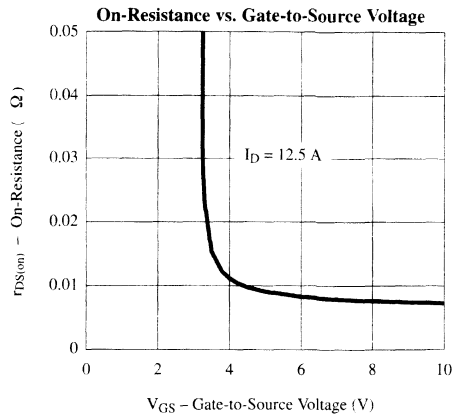
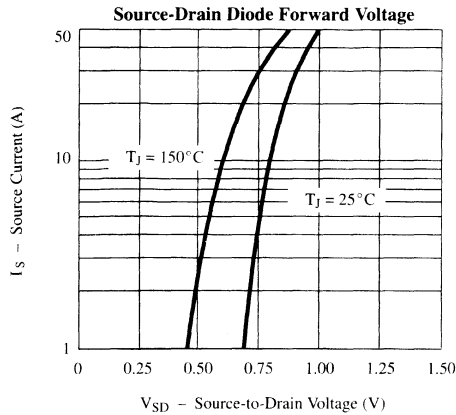
Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

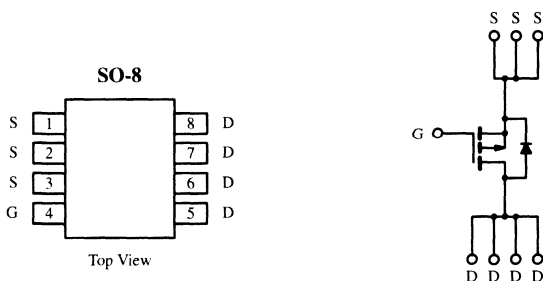


P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.014 @ $V_{GS} = -10$ V	± 11
	0.023 @ $V_{GS} = -4.5$ V	± 8.5

TrenchFET™
Power MOSFETs



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70641.

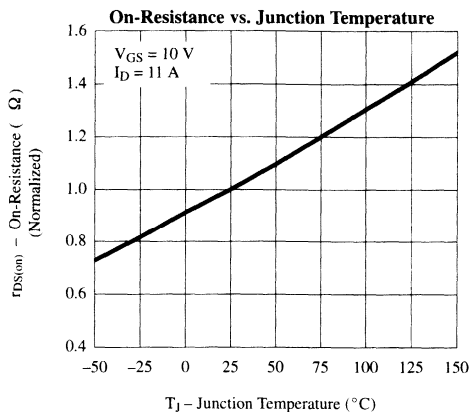
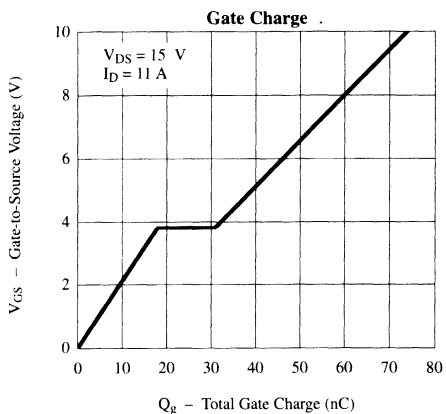
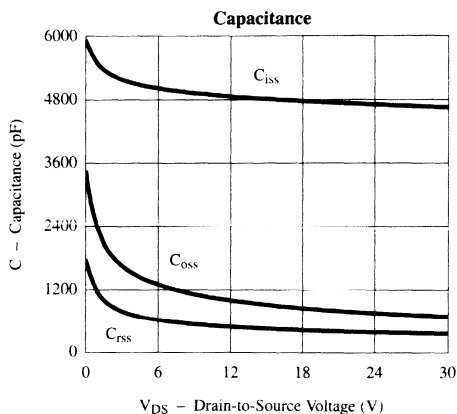
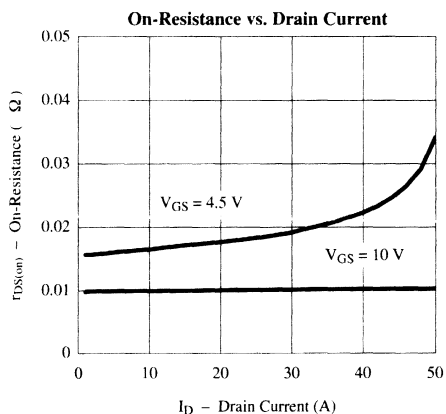
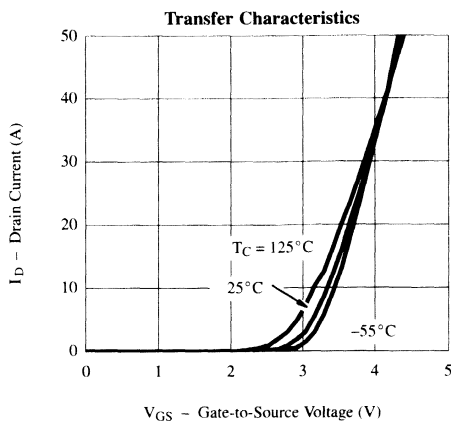
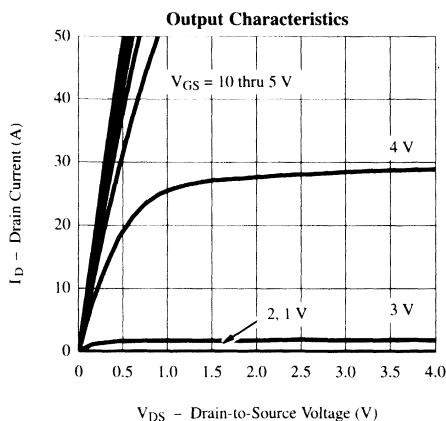
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -10\ \text{V}$	30			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}$, $I_D = -11\ \text{A}$		0.010	0.014	Ω
		$V_{GS} = -4.5\ \text{V}$, $I_D = -8.5\ \text{A}$		0.017	0.023	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -11\ \text{A}$		37		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.1\ \text{A}$, $V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}$, $V_{GS} = -10\ \text{V}$, $I_D = -11\ \text{A}$		74	120	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			13		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \approx -1\ \text{A}$, $V_{GEN} = -10\ \text{V}$, $R_G = 6\ \Omega$		16	25	ns
Rise Time	t_r			11	25	
Turn-Off Delay Time	$t_{d(off)}$			122	200	
Fall Time	t_f			40	80	
Source-Drain Reverse Recovery Time	t_{rr}			49	90	

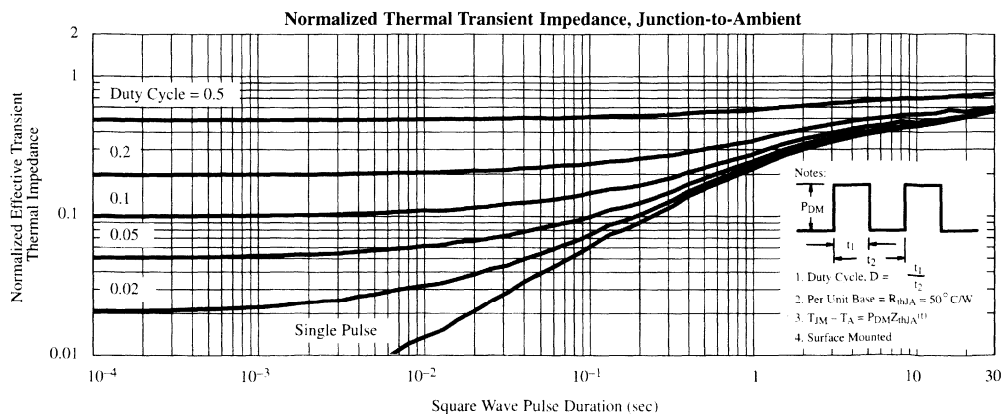
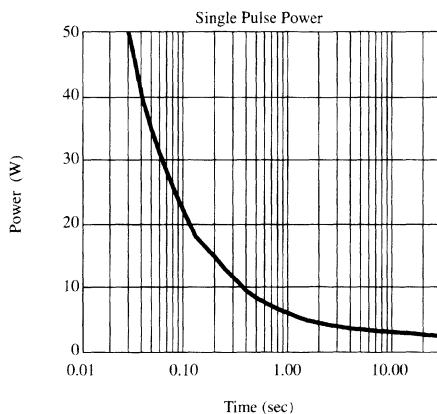
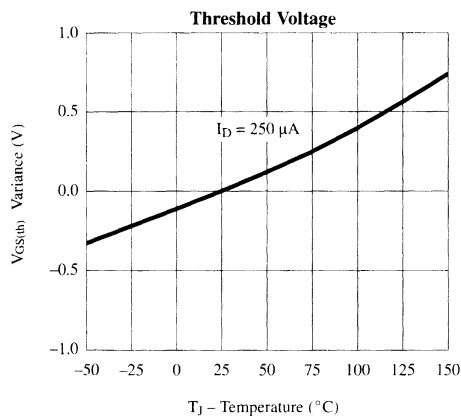
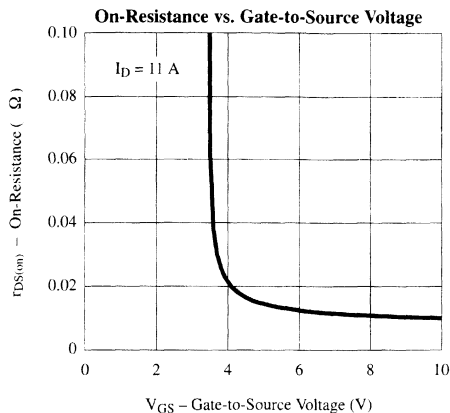
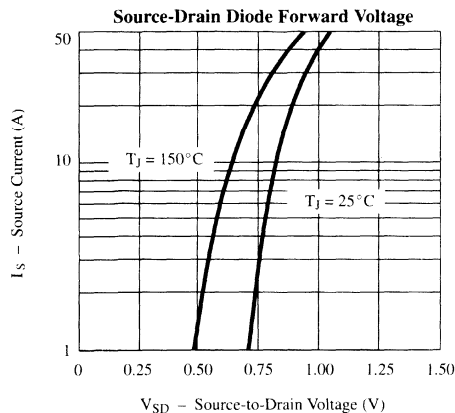
Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



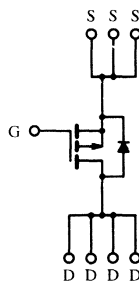
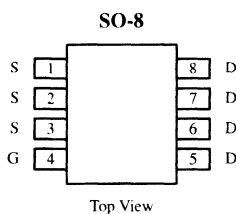
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SOIC-8

Typical Characteristics (25°C Unless Otherwise Noted)


P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-30	0.02 @ V _{GS} = -10 V	± 8.0
	0.035 @ V _{GS} = -4.5 V	± 6.0



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25° C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	-30	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150° C) ^a	T _A = 25° C	I _D	± 8.0	A
	T _A = 70° C		± 6.4	
Pulsed Drain Current		I _{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I _S	-2.1	W
Maximum Power Dissipation ^a	T _A = 25° C	P _D	2.5	
	T _A = 70° C		1.6	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	50	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70149. A SPICE Model data sheet is available for this product (FaxBack document #70544).

Specifications (T_J = 25°C Unless Otherwise Noted)

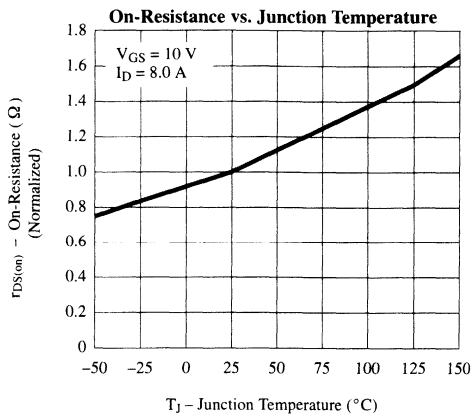
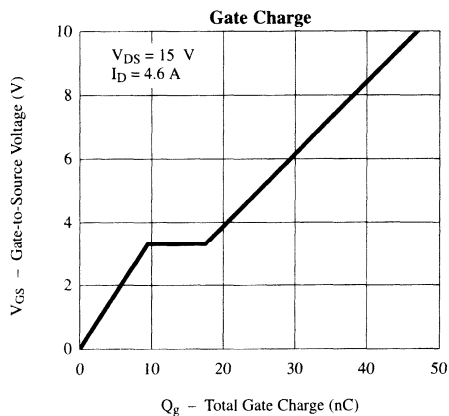
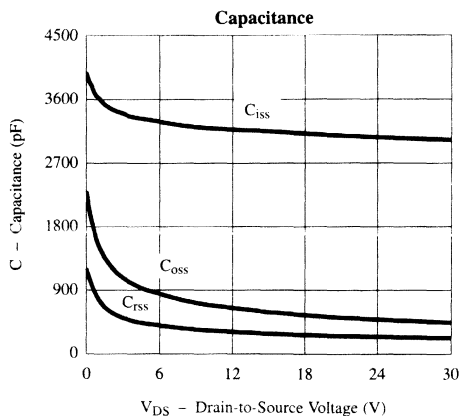
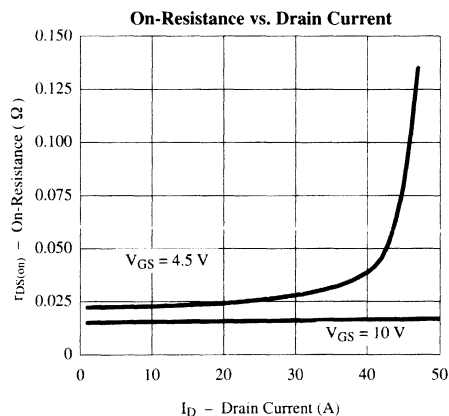
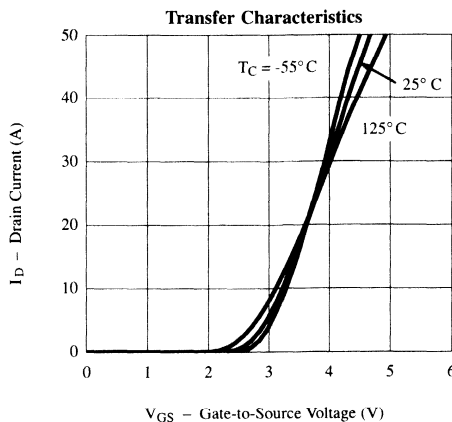
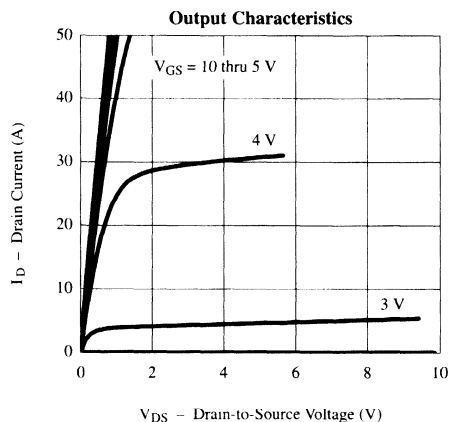
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -15 V, V _{GS} = 0 V, T _J = 70°C			-5	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-40			A
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-10			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -10 V, I _D = -8.0 A		0.015	0.02	Ω
		V _{GS} = -4.5 V, I _D = -5.0 A		0.022	0.035	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -8.0 A		20		S
Diode Forward Voltage ^b	V _{SD}	I _S = -2.1 A, V _{GS} = 0 V		-0.75	-1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -4.6 A		47	60	nC
Gate-Source Charge	Q _{gs}			9.5		
Gate-Drain Charge	Q _{gd}			8		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D = -1 A, V _{GEN} = -10 V, R _G = 6 Ω		16	30	ns
Rise Time	t _r			17	30	
Turn-Off Delay Time	t _{d(off)}			75	120	
Fall Time	t _f			31	80	
Source-Drain Reverse Recovery Time	t _{rr}			40	80	

Notes

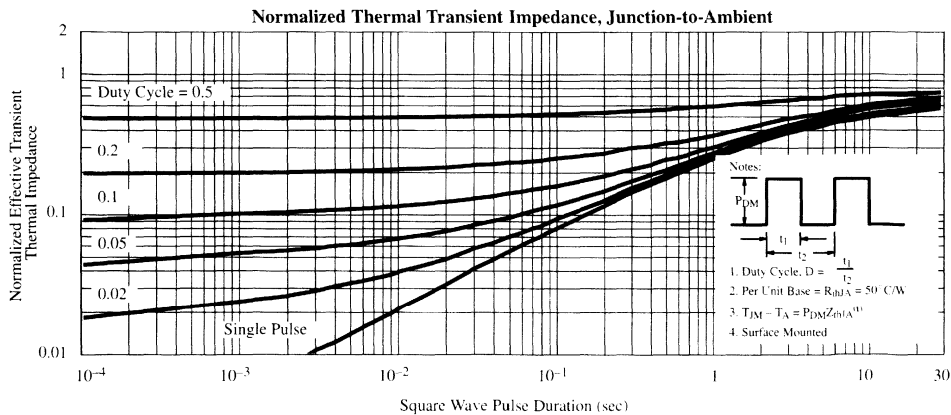
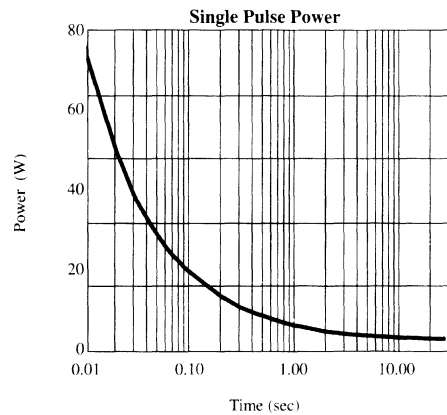
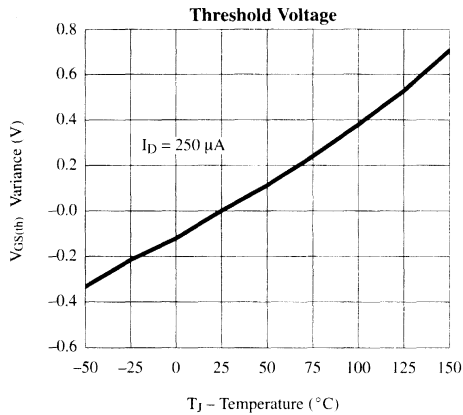
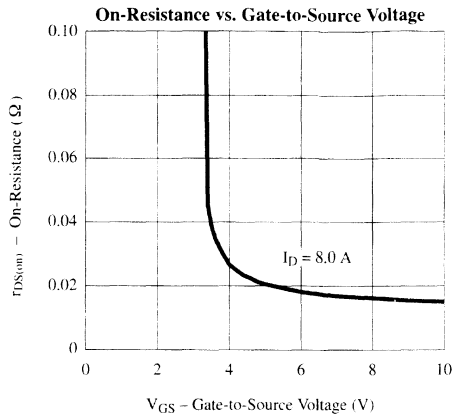
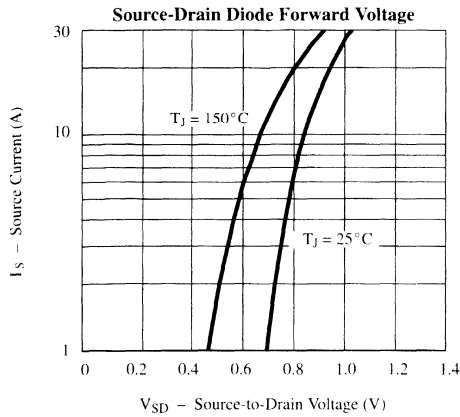
a. Guaranteed by design, not subject to production testing. Values shown are for Product Revision A.

b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Typical Characteristics, Product Revision A (25° C Unless Noted)



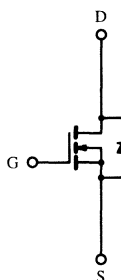
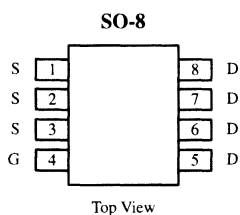
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SOIC-8

Typical Characteristics, Product Revision A (25°C Unless Noted)


N-Channel 60-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.024 @ $V_{GS} = 10$ V	± 7.5
	0.03 @ $V_{GS} = 6.0$ V	± 6.5



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$ ± 7.5	A
		$T_A = 70^\circ\text{C}$ ± 5.5	
Pulsed Drain Current	I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$ 2.5	W
		$T_A = 70^\circ\text{C}$ 1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70144.

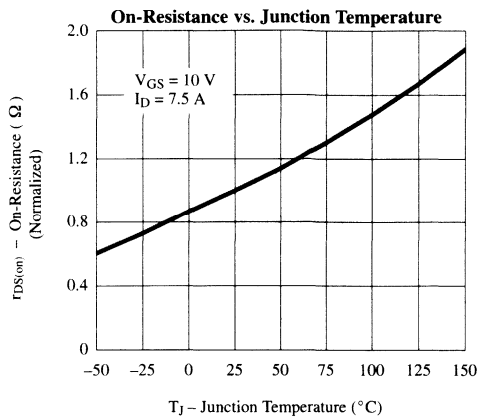
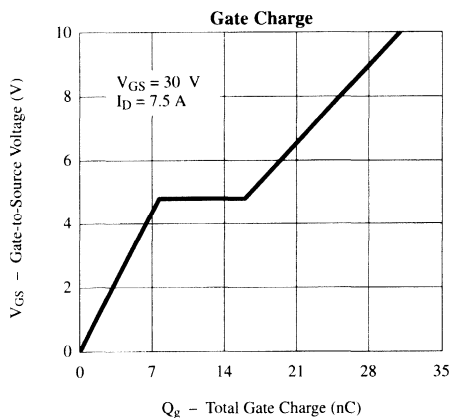
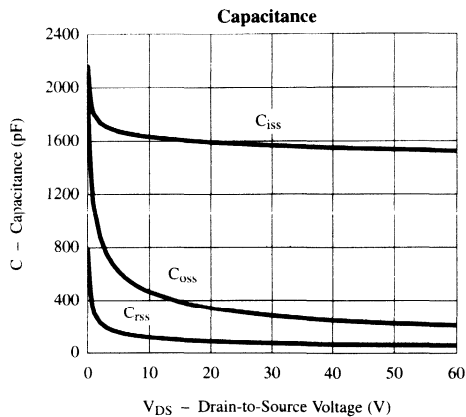
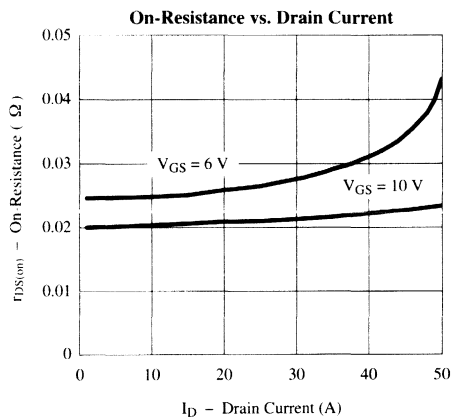
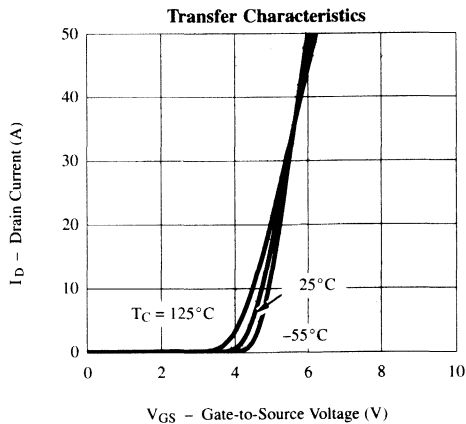
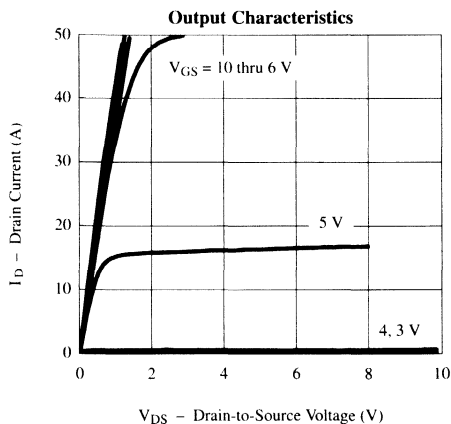
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 7.5\ \text{A}$		0.020	0.024	Ω
		$V_{GS} = 6.0\ \text{V}$, $I_D = 6.5\ \text{A}$		0.025	0.03	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 7.5\ \text{A}$		18.5		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.75	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 30\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 7.5\ \text{A}$		31	50	nC
Gate-Source Charge	Q_{gs}			7.7		
Gate-Drain Charge	Q_{gd}			8.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\ \text{V}$, $R_L = 30\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			41	80	
Fall Time	t_f			21	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		46	80	

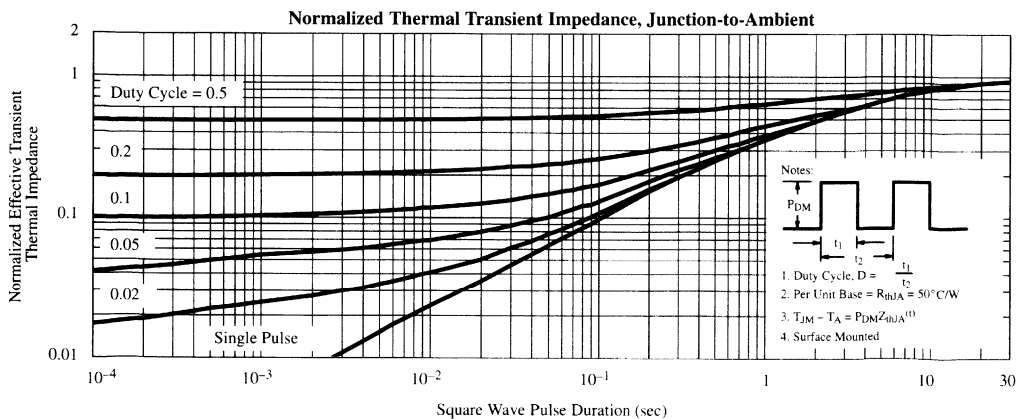
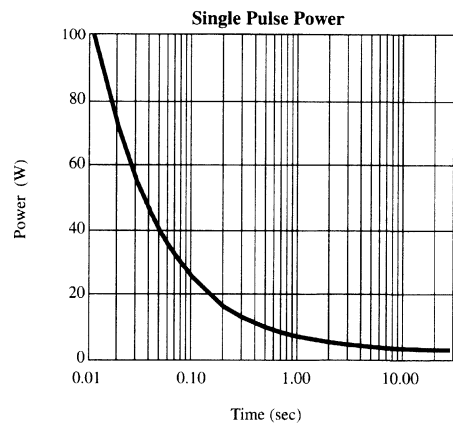
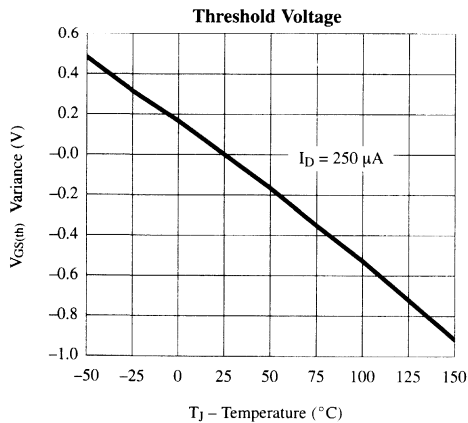
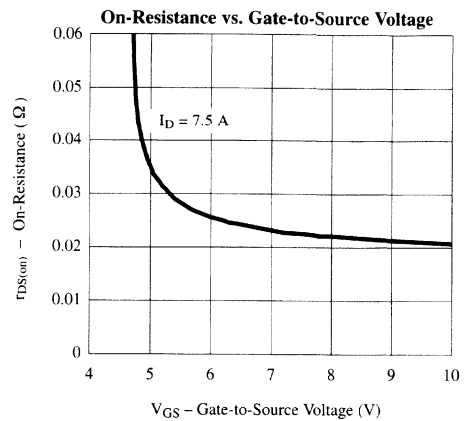
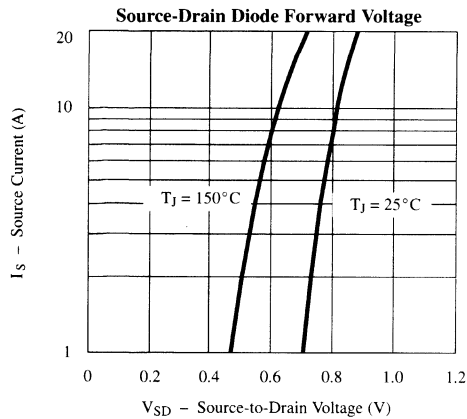
Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

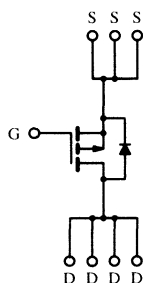
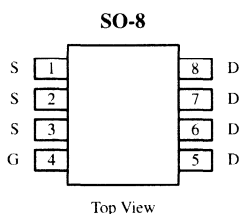


P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.014 @ $V_{GS} = -4.5$ V	± 10
	0.0200 @ $V_{GS} = -2.5$ V	± 8.8

TrenchFET™
Power MOSFETs
2.5-V Rated



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$ ± 10	A
		$T_A = 70^\circ\text{C}$ ± 8.3	
Pulsed Drain Current	I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$ 2.5	W
		$T_A = 70^\circ\text{C}$ 1.6	
Operating Junction and Storage Temperature Range	T_J, T_{sig}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70707.

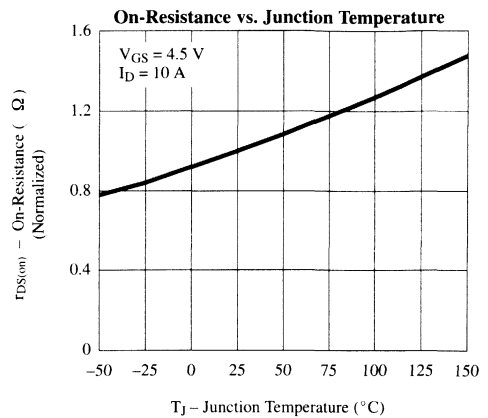
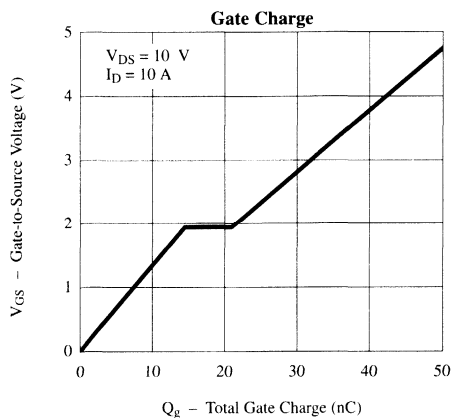
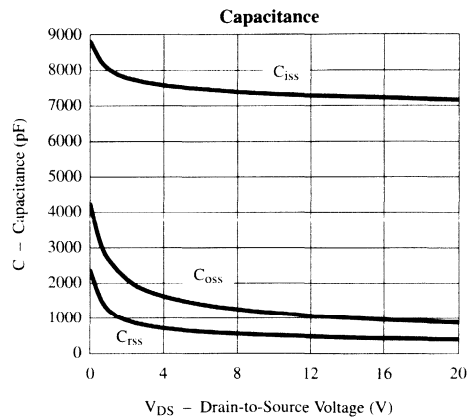
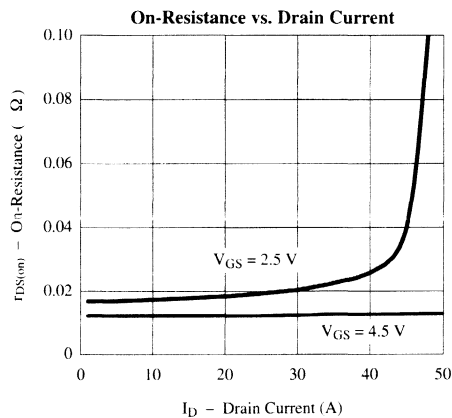
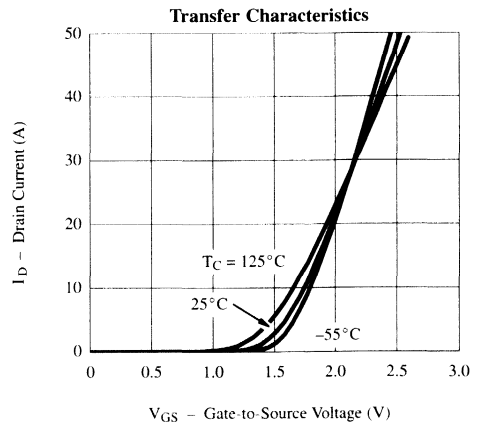
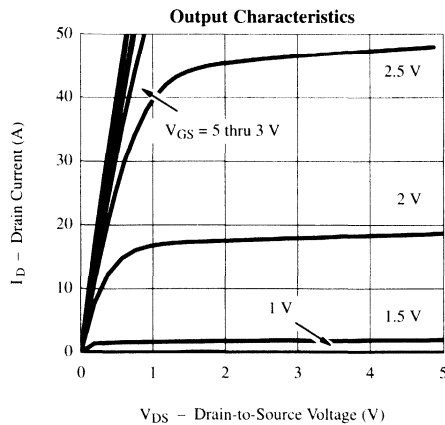
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -10\ \text{A}$		0.012	0.014	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -8.8\ \text{A}$		0.017	0.0200	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -10\ \text{A}$		40		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.1\ \text{A}, V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -10\ \text{A}$		48	70	nC
Gate-Source Charge	Q_{gs}			15		
Gate-Drain Charge	Q_{gd}			7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \approx -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		40	60	ns
Rise Time	t_r			40	60	
Turn-Off Delay Time	$t_{d(off)}$			190	280	
Fall Time	t_f			95	140	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		45	80	

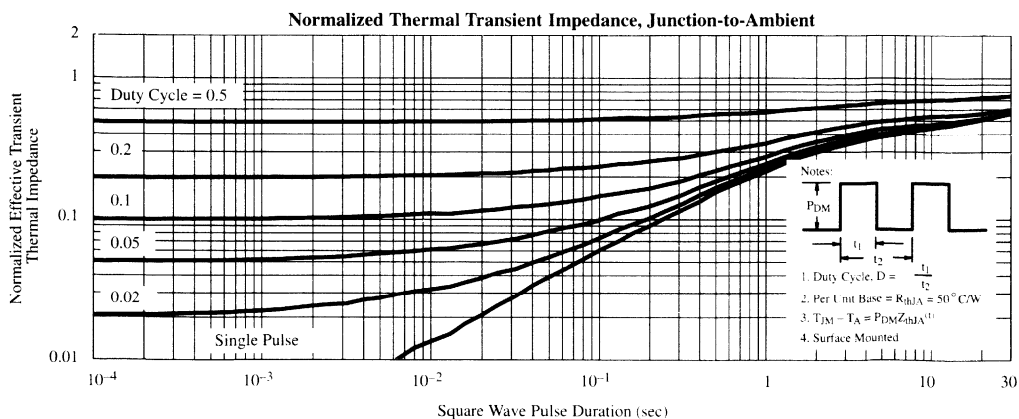
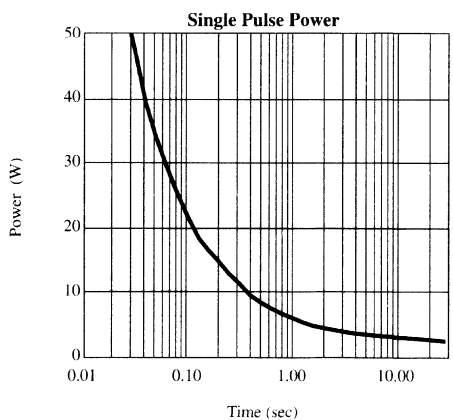
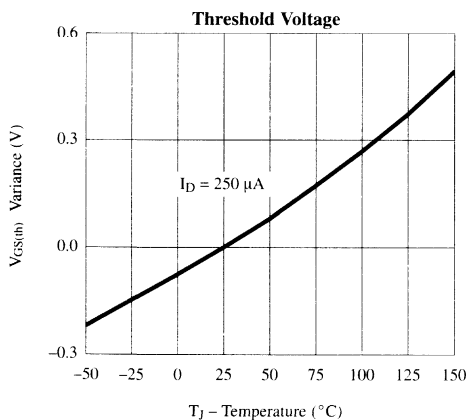
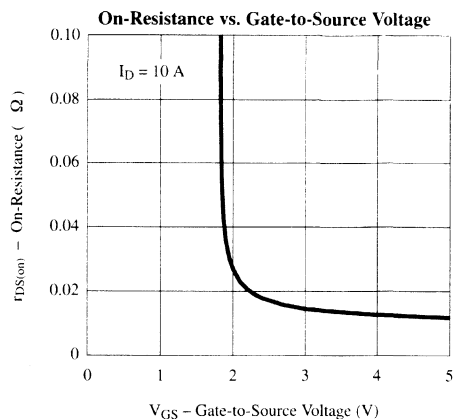
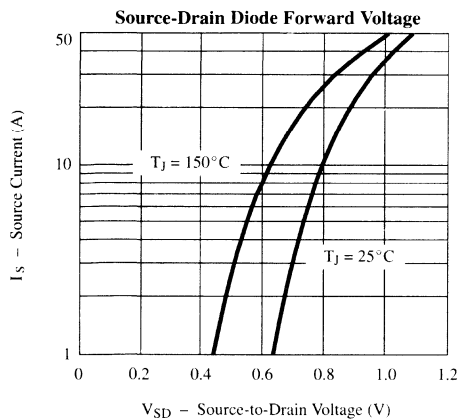
Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

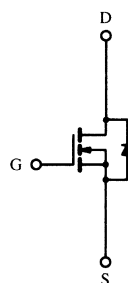
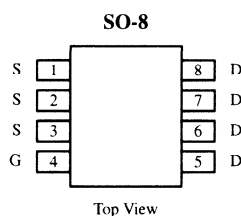


N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.009 @ $V_{GS} = 4.5$ V	± 13.2
	0.013 @ $V_{GS} = 2.5$ V	± 11

TrenchFET™
Power MOSFETs
2.5-V Rated



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 13.2	A
	$T_A = 70^\circ\text{C}$		± 10.5	
Pulsed Drain Current		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	2.3	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70716.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

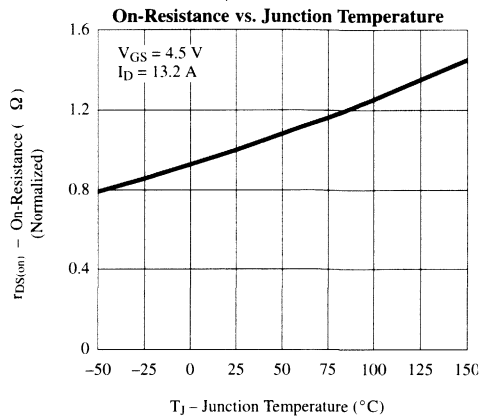
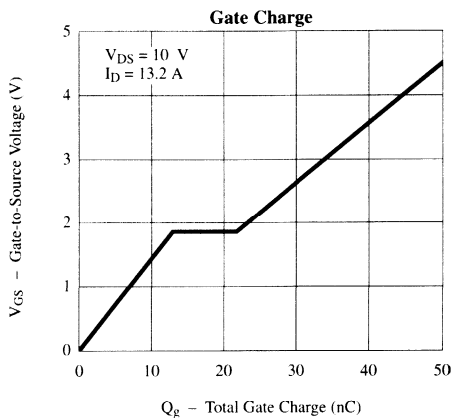
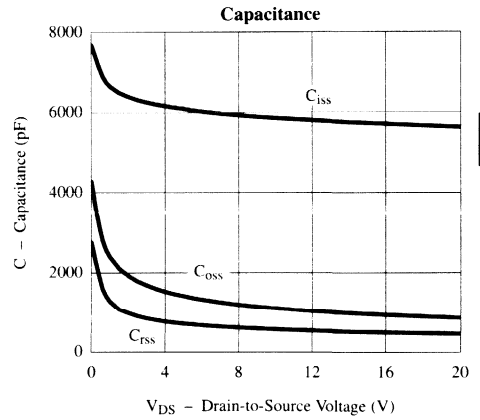
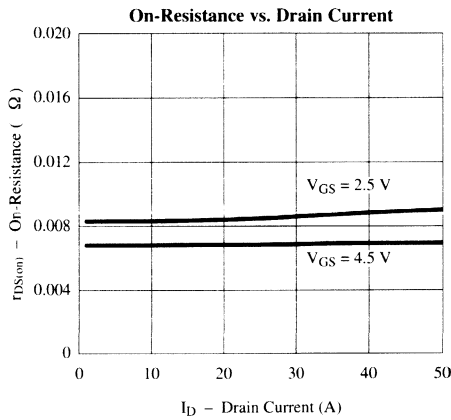
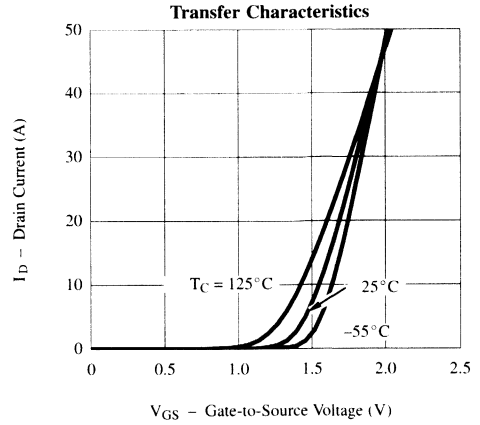
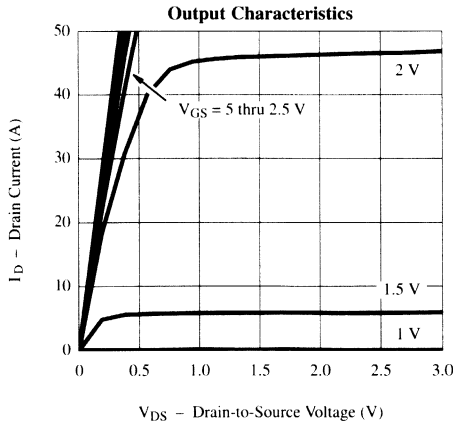
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 4.5\ \text{V}$	30			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}$, $I_D = 13.2\ \text{A}$		0.007	0.009	Ω
		$V_{GS} = 2.5\ \text{V}$, $I_D = 11\ \text{A}$		0.0085	0.013	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 13.2\ \text{A}$		60		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.3\ \text{A}$, $V_{GS} = 0\ \text{V}$			1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 13.2\ \text{A}$		50	80	nC
Gate-Source Charge	Q_{gs}			13		
Gate-Drain Charge	Q_{gd}			9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \approx 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		40	60	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			210	280	
Fall Time	t_f			85	140	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		55	90	

Notes

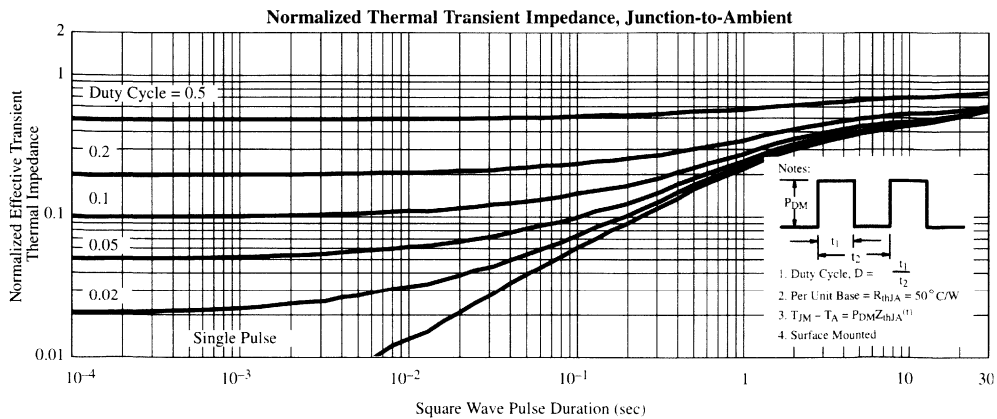
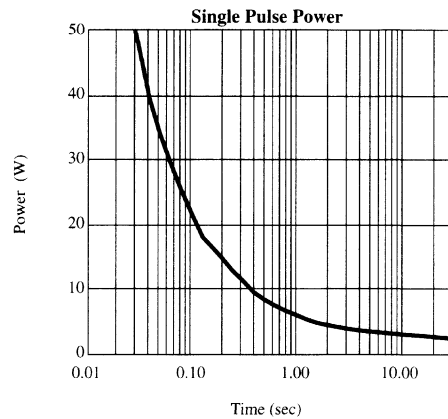
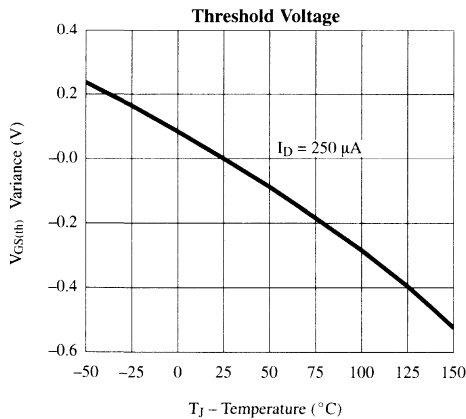
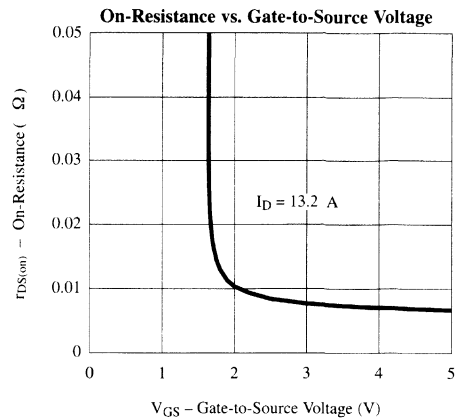
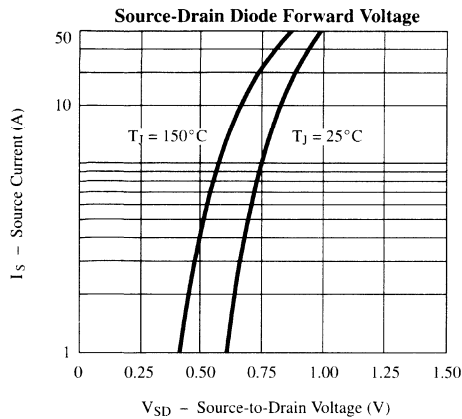
a. Guaranteed by design, not subject to production testing.

 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

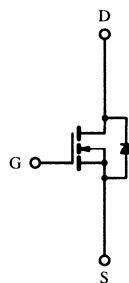
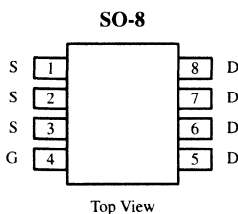


N-Channel 80-V Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.035 @ $V_{GS} = 10$ V	± 6.0
	0.040 @ $V_{GS} = 6.0$ V	± 5.5

TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 6.0	A
		± 48	
Pulsed Drain Current	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	
Maximum Power Dissipation ^a	P_D	2.5	W
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70645.

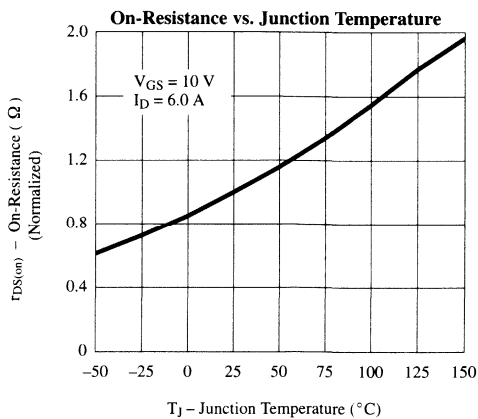
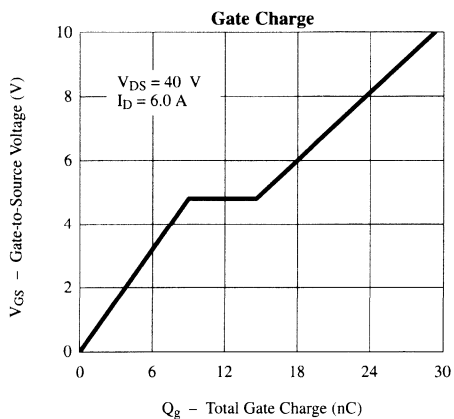
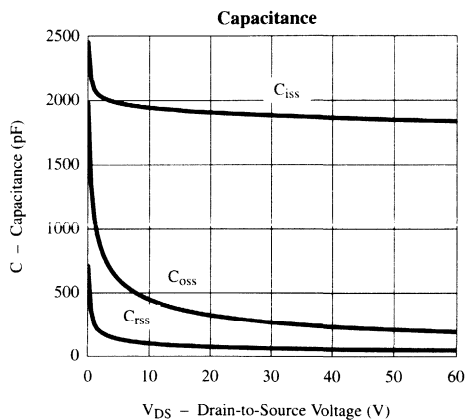
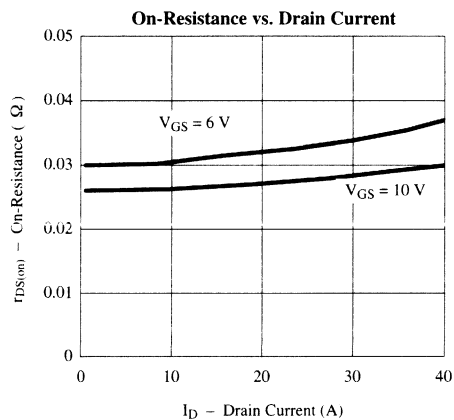
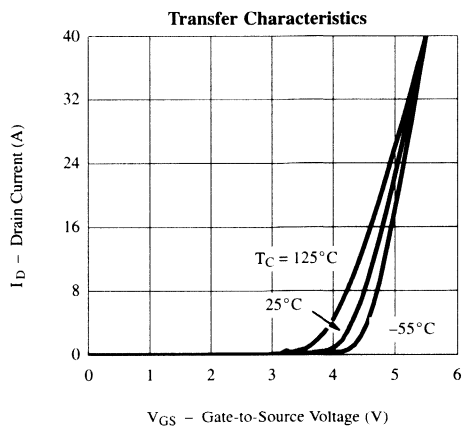
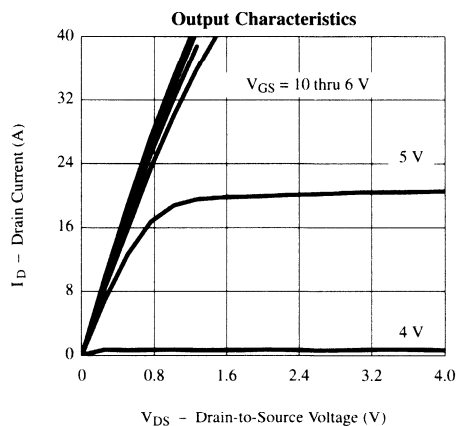
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 6.0\ \text{A}$		0.026	0.035	Ω
		$V_{GS} = 6.0\ \text{V}$, $I_D = 5.5\ \text{A}$		0.030	0.040	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 6.0\ \text{A}$		25		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\ \text{A}$, $V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 40\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 6.0\ \text{A}$		30	50	nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			5.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\ \text{V}$, $R_L = 30\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		12.5	25	ns
Rise Time	t_r			12.5	25	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			22	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

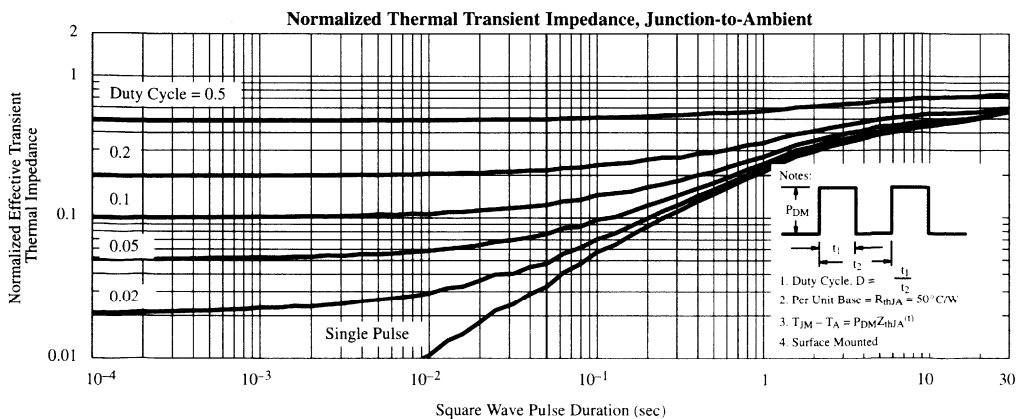
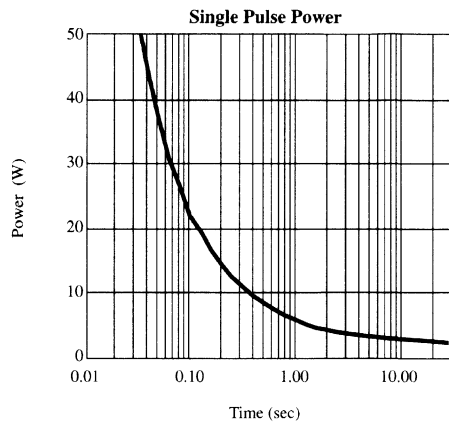
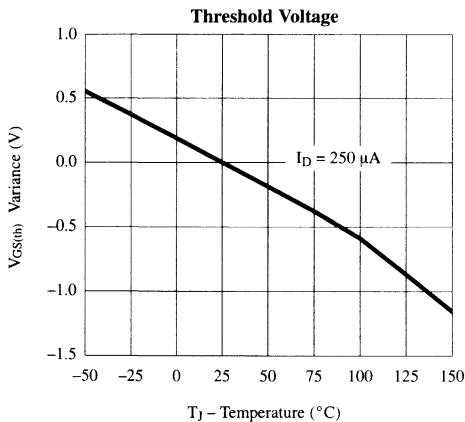
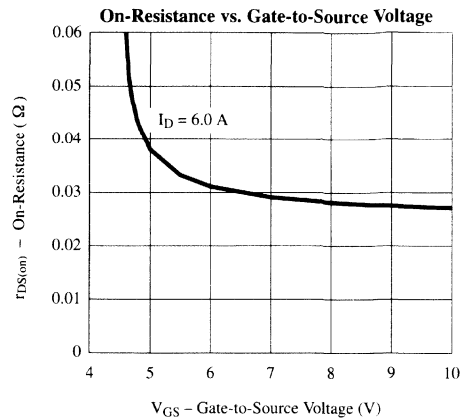
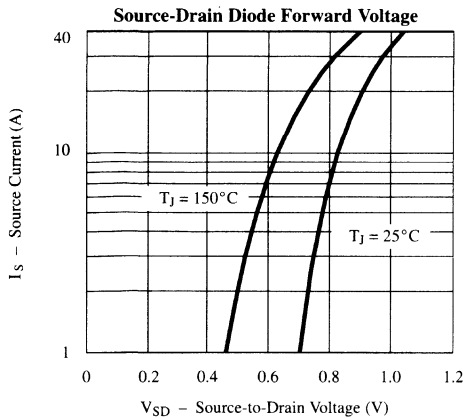
Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

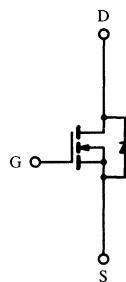
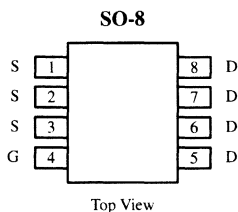


N-Channel 100-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.060 @ $V_{GS} = 10$ V	± 4.6
	0.080 @ $V_{GS} = 6$ V	± 4.0

TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$ ± 4.6	A
		$T_A = 70^\circ\text{C}$ ± 3.7	
Pulsed Drain Current	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$ 2.5	W
		$T_A = 70^\circ\text{C}$ 1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70749.

Specifications (T_J = 25° C Unless Otherwise Noted)

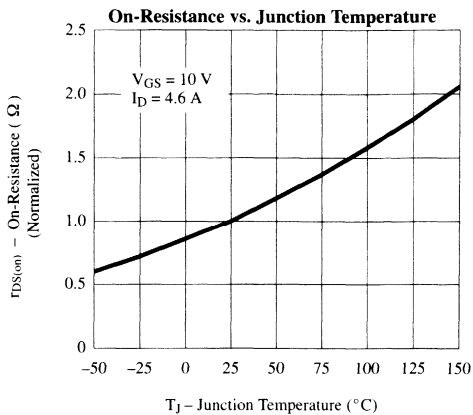
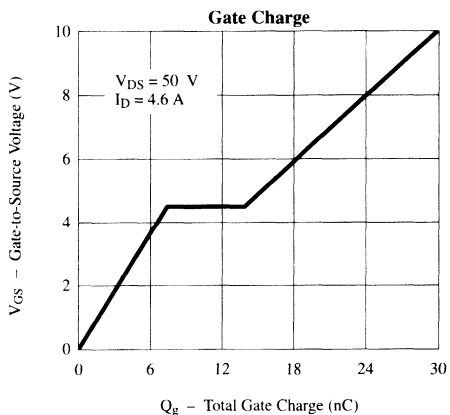
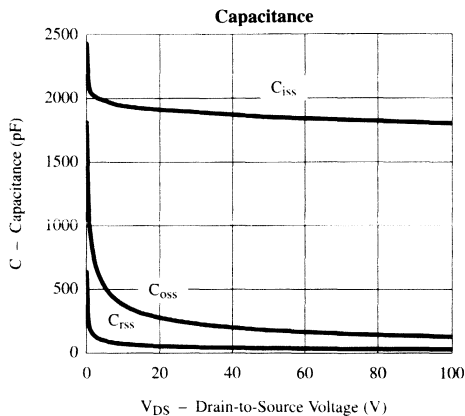
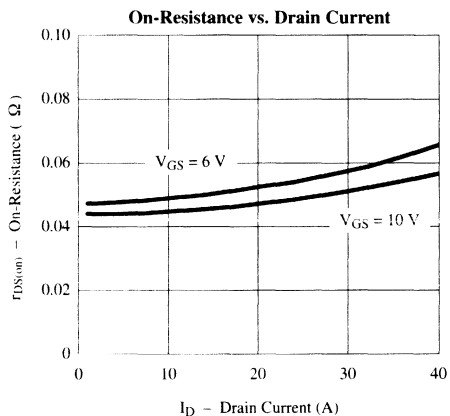
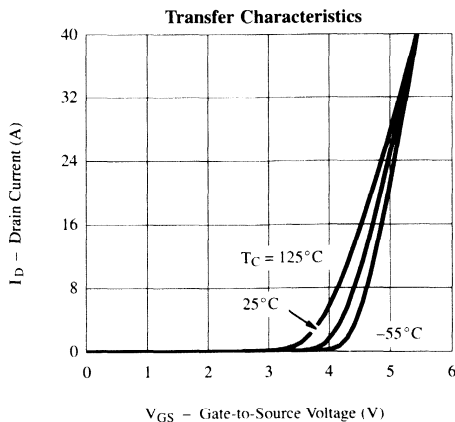
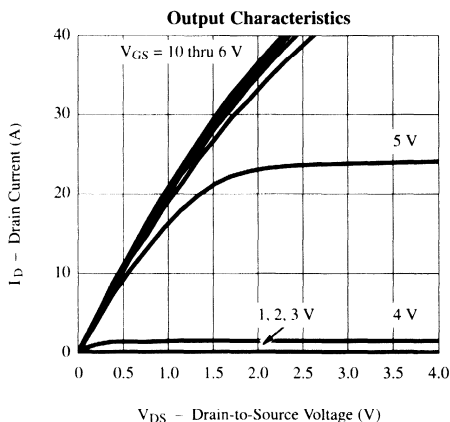
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55° C			20	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.6 A		0.045	0.060	Ω
		V _{GS} = 6 V, I _D = 4.0 A		0.050	0.080	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 4.6 A		20		S
Diode Forward Voltage ^b	V _{SD}	I _S = 2.1 A, V _{GS} = 0 V			1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 4.6 A		30	50	nC
Gate-Source Charge	Q _{gs}			7.5		
Gate-Drain Charge	Q _{gd}			7		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D = 1 A, V _{GEN} = 10 V, R _G = 6 Ω		13	25	ns
Rise Time	t _r			12	25	
Turn-Off Delay Time	t _{d(off)}			60	90	
Fall Time	t _f			25	40	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.1 A, di/dt = 100 A/μs		50	80	

Notes

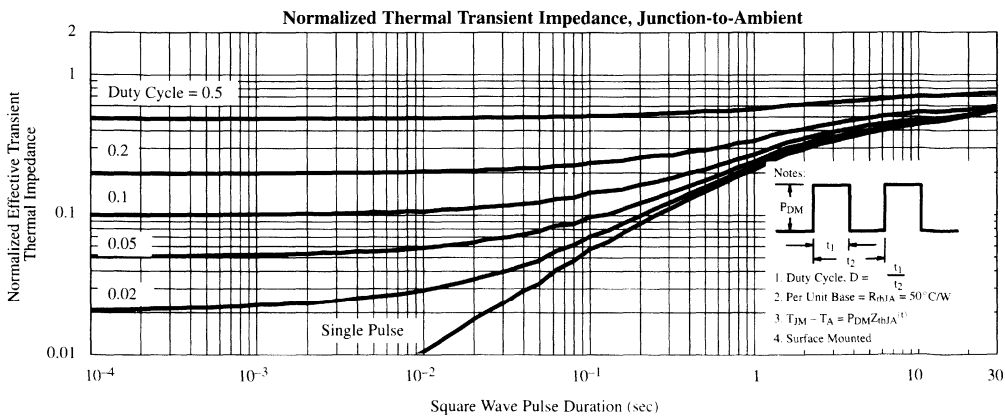
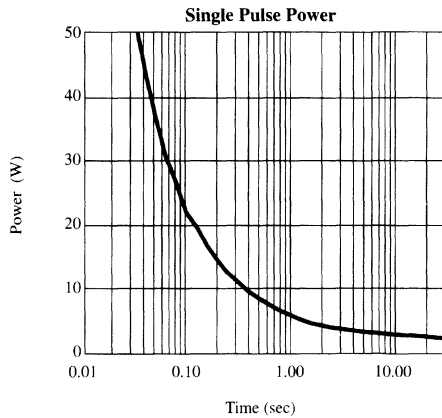
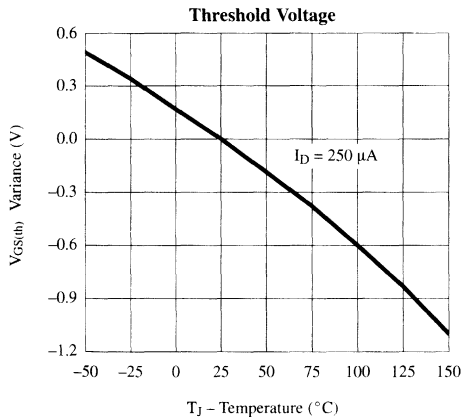
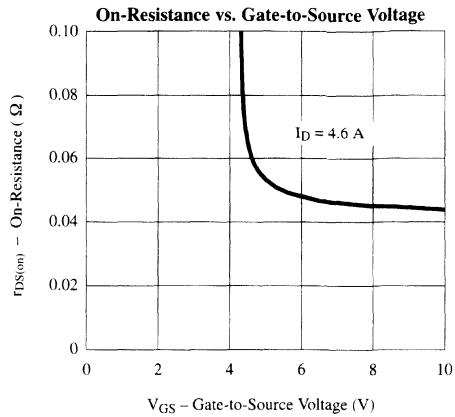
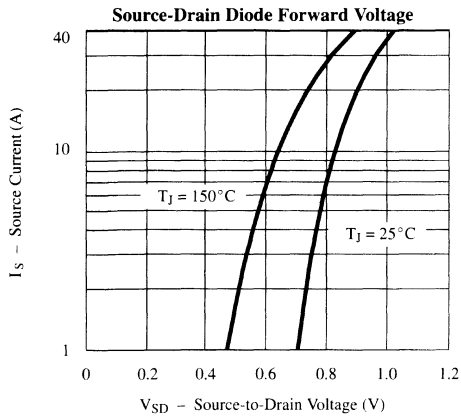
a. For design aid only; not subject to production testing.

b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)



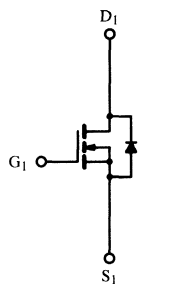
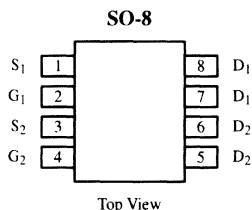
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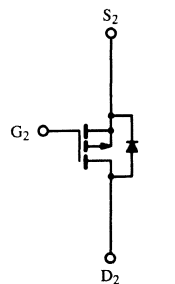
Dual N- and P-Channel 30-V (D-S) Rated MOSFET

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.065 @ $V_{GS} = 10$ V	± 3.9
		0.095 @ $V_{GS} = 4.5$ V	± 3.1
P-Channel	-30	0.085 @ $V_{GS} = -10$ V	± 3.5
		0.19 @ $V_{GS} = -4.5$ V	± 2.5



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	
Continuous Drain Current ($T_J = 150^{\circ}\text{C}$) ^a	$T_A = 25^{\circ}\text{C}$	I_D	± 3.9	± 3.5	A
	$T_A = 70^{\circ}\text{C}$		± 3.1	± 2.8	
Pulsed Drain Current		I_{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^a		I_S	1.7	-1.7	
Maximum Power Dissipation ^a	$T_A = 25^{\circ}\text{C}$	P_D	2.0		W
	$T_A = 70^{\circ}\text{C}$		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70155. A SPICE Model data sheet is available for this product (FaxBack document #70551)

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0		V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch P-Ch		± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{DS} = -30 V, V _{GS} = 0 V	P-Ch		-1		
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55°C	N-Ch		25		
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55°C	P-Ch		-25		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	15		A	
		V _{DS} ≥ -5 V, V _{GS} = -10 V	P-Ch	-15			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 3.9 A	N-Ch		0.043	Ω	
		V _{GS} = -10 V, I _D = 2.5 A	P-Ch		0.066		
		V _{GS} = 4.5 V, I _D = 3.1 A	N-Ch		0.075		
		V _{GS} = -4.5 V, I _D = 1.8 A	P-Ch		0.125		
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3.9 A	N-Ch		7	S	
		V _{DS} = -15 V, I _D = -2.5 A	P-Ch		5		
Diode Forward Voltage ^b	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch		0.8	V	
		I _S = -1.7 A, V _{GS} = 0 V	P-Ch		-0.8		
Dynamic ^a							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 3.9 A P-Channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -2.5 A	N-Ch		9.8	15	nC
Gate-Source Charge	Q _{gs}		P-Ch		8.7	15	
			N-Ch		2.1		
Gate-Drain Charge	Q _{gd}		P-Ch		1.9		
		N-Ch		1.6			
Turn-On Delay Time	t _{d(on)}	P-Ch		1.3			
		N-Ch		9	15		
Rise Time	t _r	P-Ch		7	15		
		N-Ch		6	18		
Turn-Off Delay Time	t _{d(off)}	P-Ch		9	18		
		N-Ch		18	27		
Fall Time	t _f	P-Ch		14	27		
		N-Ch		6	15		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		52	80	
		I _F = -1.7 A, di/dt = 100 A/μs	P-Ch		50	80	

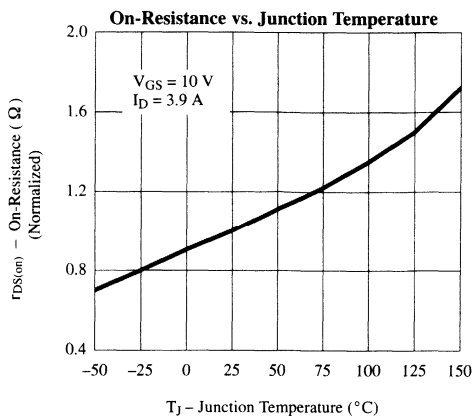
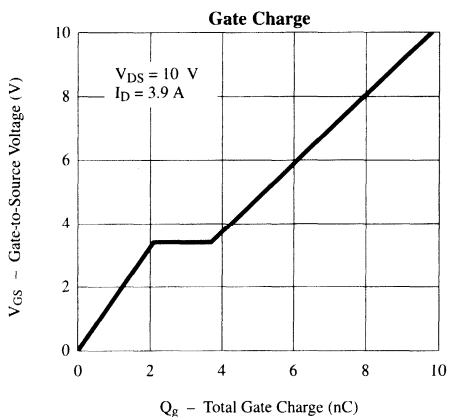
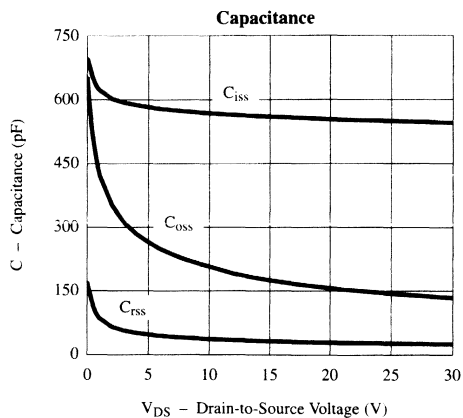
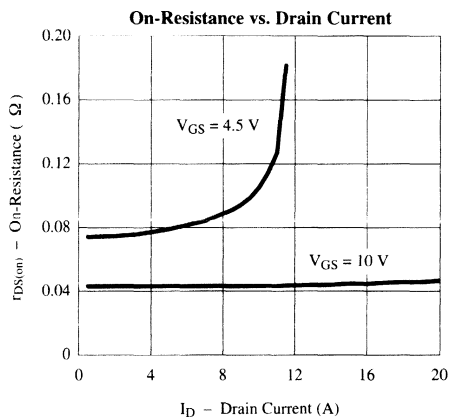
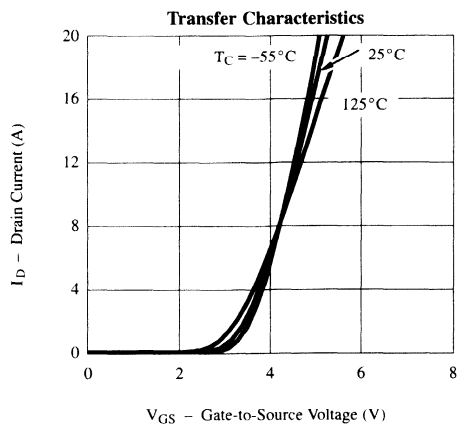
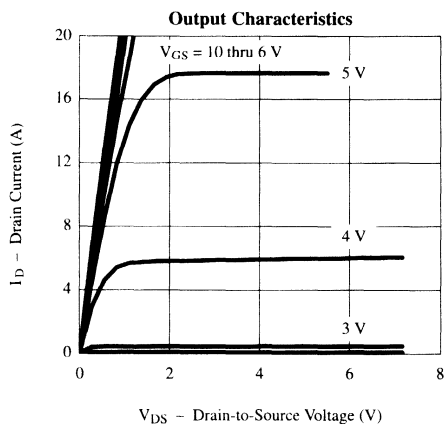
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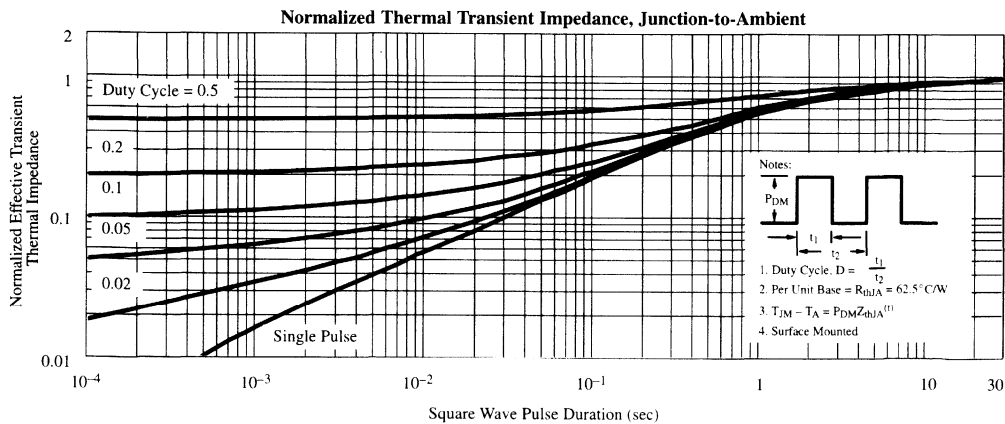
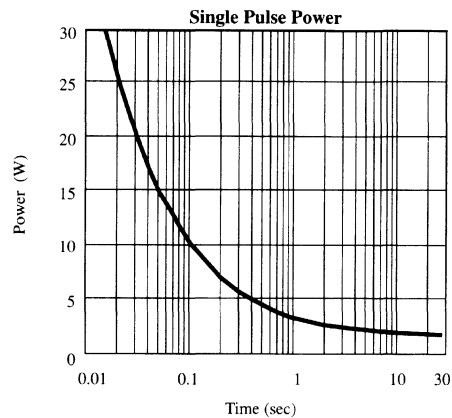
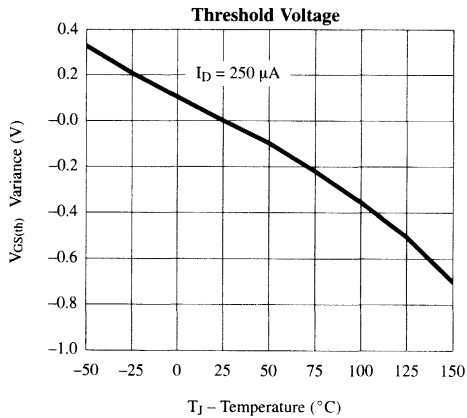
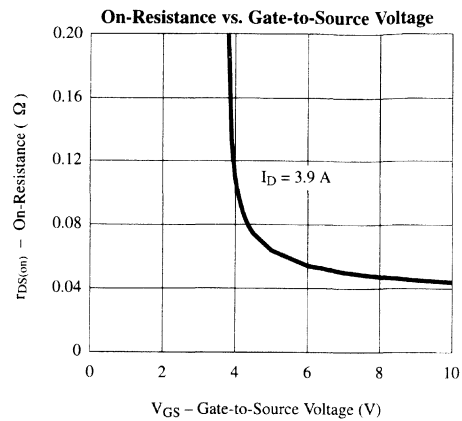
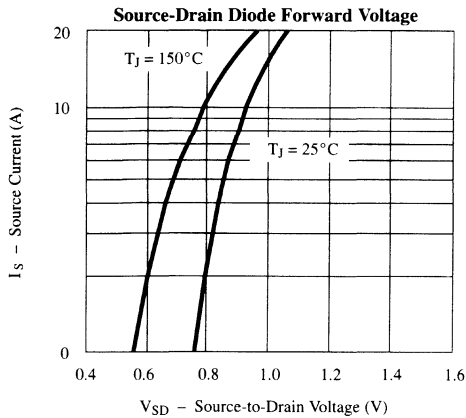
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Noted)

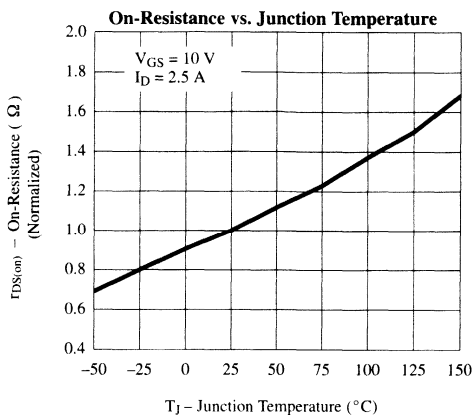
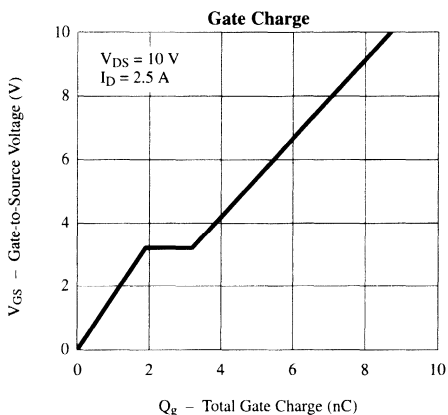
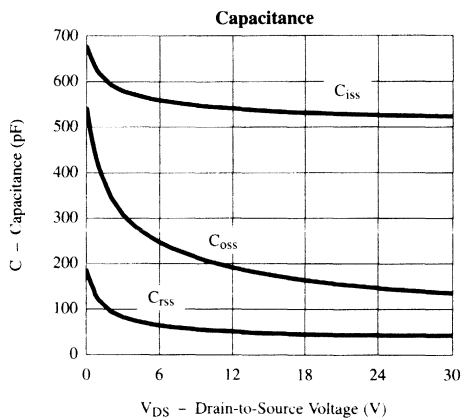
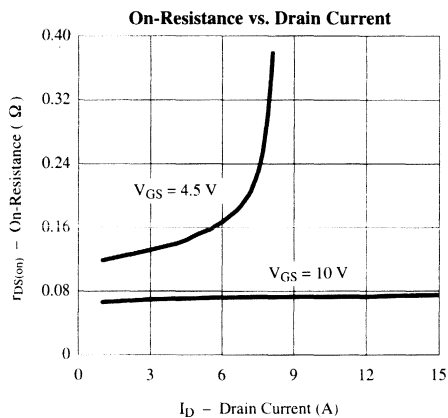
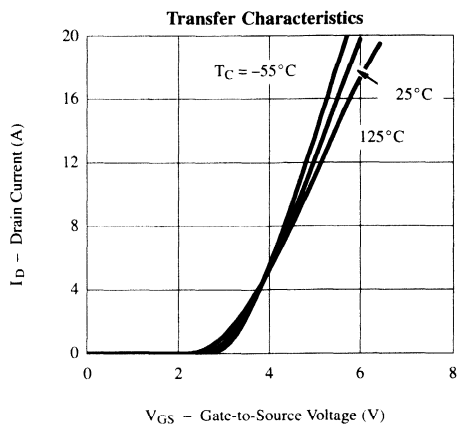
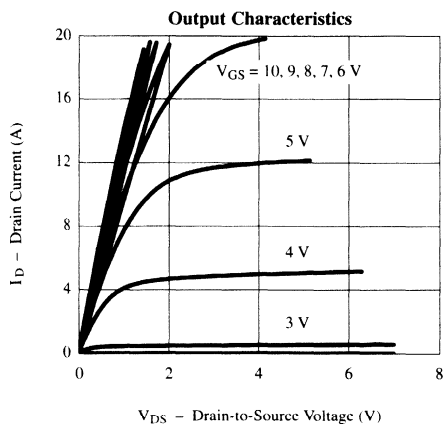
N-Channel



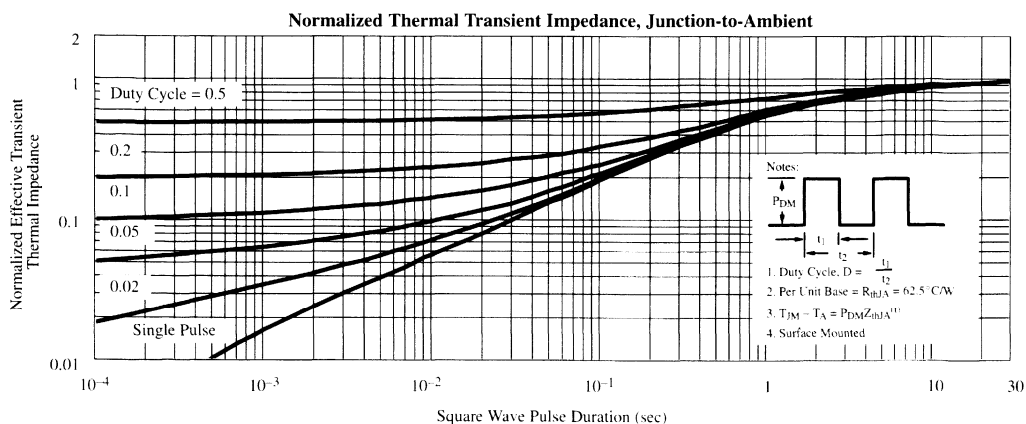
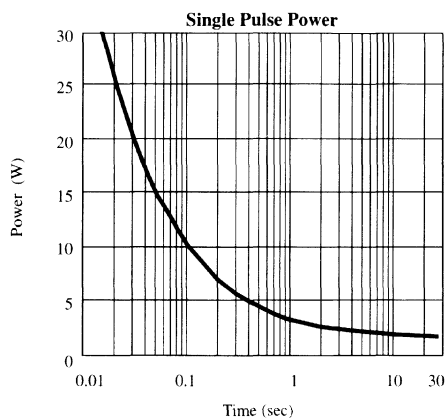
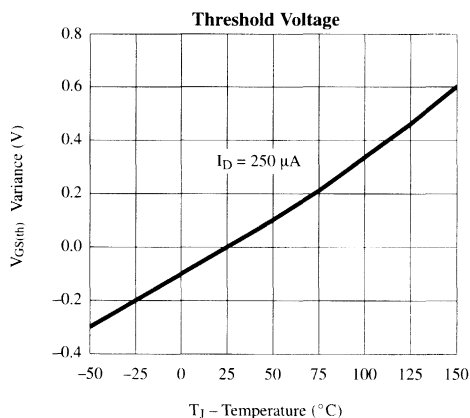
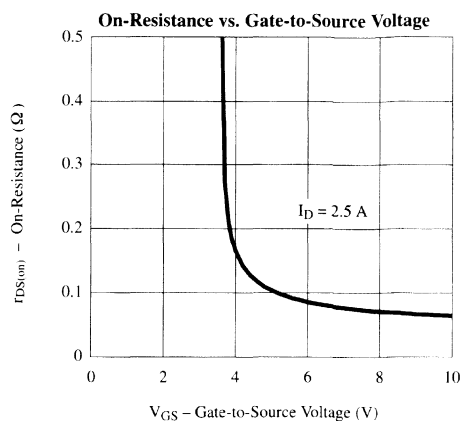
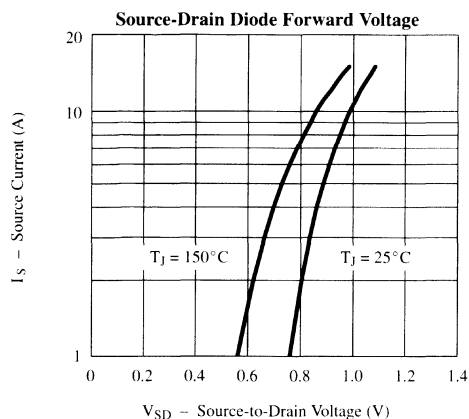
Typical Characteristics (25°C Unless Noted)
N-Channel


Typical Characteristics (25°C Unless Noted)

P-Channel



3
SOIC-8

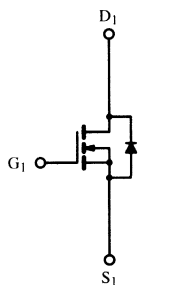
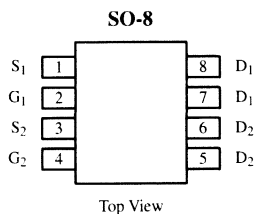
Typical Characteristics (25°C Unless Noted)
P-Channel


Dual N- and P-Channel 30-V (D-S) Rated MOSFET

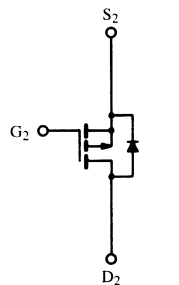
Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	30	0.025 @ V _{GS} = 10 V	± 6.9
		0.035 @ V _{GS} = 4.5 V	± 5.8
P-Channel	-30	0.032 @ V _{GS} = -10 V	± 6.1
		0.045 @ V _{GS} = -4.5 V	± 5.1

TrenchFET™
Power MOSFETs



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	30	−30	V
Gate-Source Voltage		V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	± 6.9	± 6.1	A
	T _A = 70 °C		± 5.5	± 4.9	
Pulsed Drain Current		I _{DM}	± 40	± 40	
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	−1.7	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.0		W
	T _A = 70 °C		1.3		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70666.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	N-Ch	1.0		V	
		$V_{DS} = V_{GS}, I_D = -250\ \mu A$	P-Ch	-1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V, V_{GS} = \pm 20\ V$	N-Ch P-Ch		± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ V, V_{GS} = 0\ V$	N-Ch		1	μA	
		$V_{DS} = -30\ V, V_{GS} = 0\ V$	P-Ch		-1		
		$V_{DS} = 30\ V, V_{GS} = 0\ V, T_J = 55^\circ C$	N-Ch		25		
		$V_{DS} = -30\ V, V_{GS} = 0\ V, T_J = 55^\circ C$	P-Ch		-25		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ V, V_{GS} = 10\ V$	N-Ch	20		A	
		$V_{DS} \leq -5\ V, V_{GS} = -10\ V$	P-Ch	-20			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ V, I_D = 6.9\ A$	N-Ch		0.020	Ω	
		$V_{GS} = -10\ V, I_D = 6.1\ A$	P-Ch		0.026		
		$V_{GS} = 4.5\ V, I_D = 5.8\ A$	N-Ch		0.026		
		$V_{GS} = -4.5\ V, I_D = -5.1\ A$	P-Ch		0.036		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ V, I_D = 6.9\ A$	N-Ch		25	S	
		$V_{DS} = -15\ V, I_D = -6.1\ A$	P-Ch		16		
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\ A, V_{GS} = 0\ V$	N-Ch		1.2	V	
		$I_S = -1.7\ A, V_{GS} = 0\ V$	P-Ch		-1.2		
Dynamic ^a							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 15\ V, V_{GS} = 10\ V, I_D = 6.9\ A$ P-Channel $V_{DS} = -15\ V, V_{GS} = -10\ V, I_D = -6.1\ A$	N-Ch		30	50	nC
Gate-Source Charge	Q_{gs}		P-Ch		32	50	
			N-Ch		7.5		
Gate-Drain Charge	Q_{gd}		P-Ch		7.0		
		N-Ch		3.5			
Turn-On Delay Time	$t_{d(on)}$	P-Ch		5.0			
		N-Ch		12	20		
Rise Time	t_r	P-Ch		10	20		
		N-Ch		10	20		
Turn-Off Delay Time	$t_{d(off)}$	P-Ch		10	20		
		N-Ch		60	90		
Fall Time	t_f	P-Ch		55	80		
		N-Ch		15	30		
Source-Drain Reverse Recovery Time	t_{rr}	P-Ch		25	40		
		N-Ch		50	90		
		P-Ch		50	90		
		N-Ch					

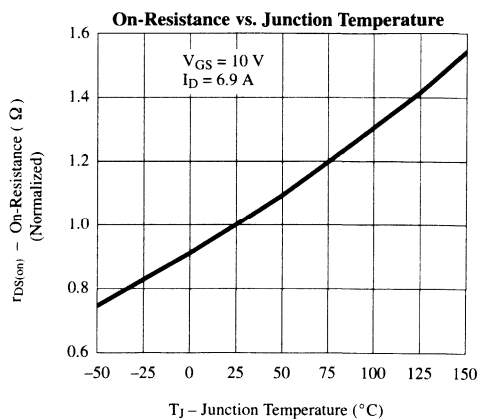
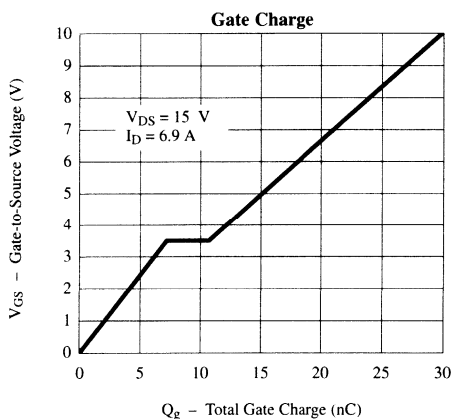
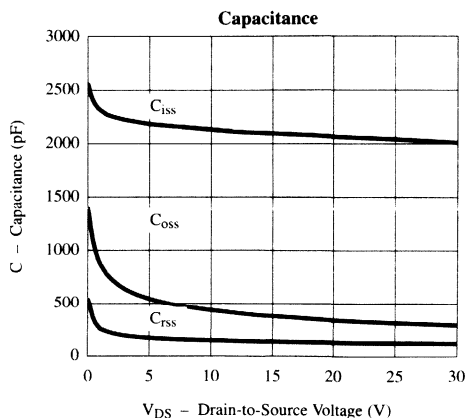
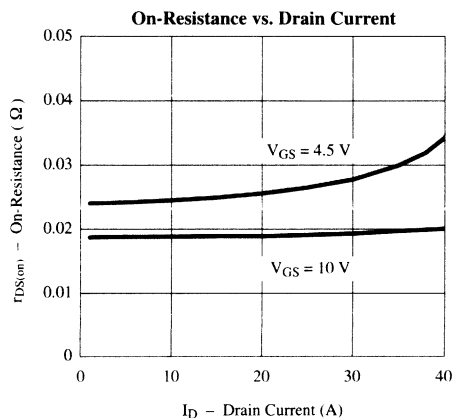
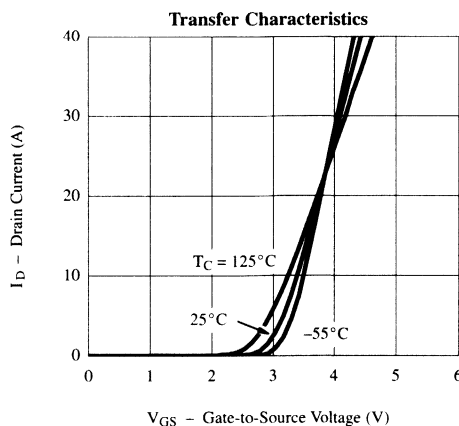
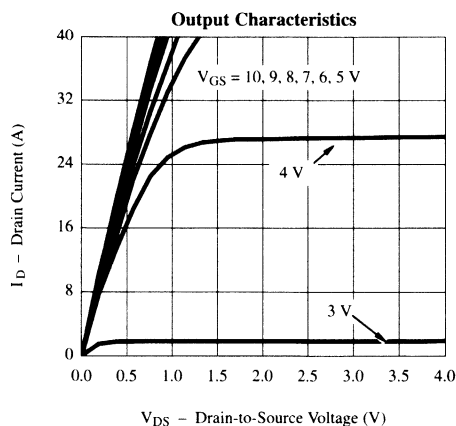
Notes

a. Guaranteed by design, not subject to production testing.

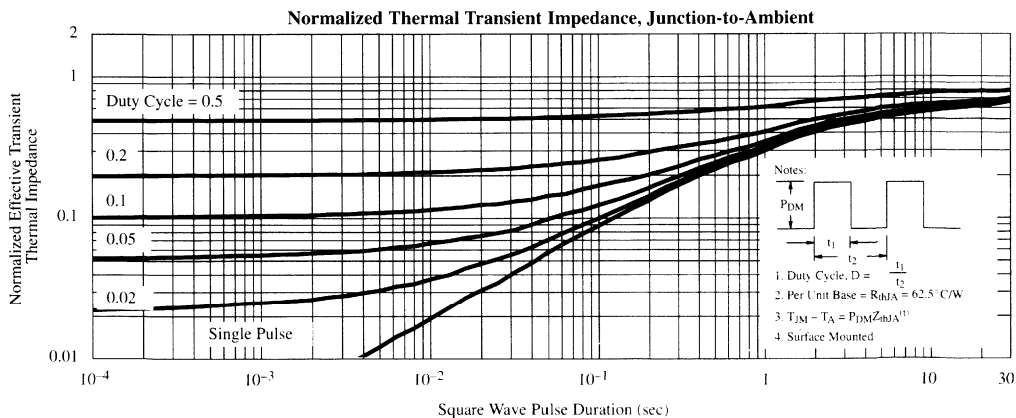
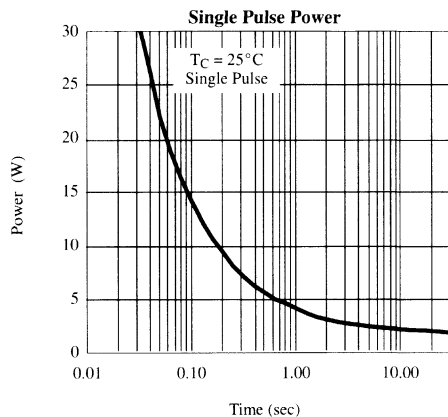
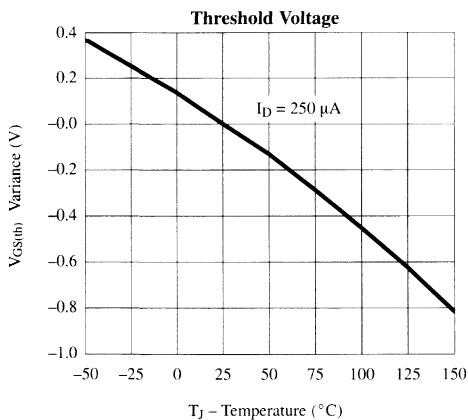
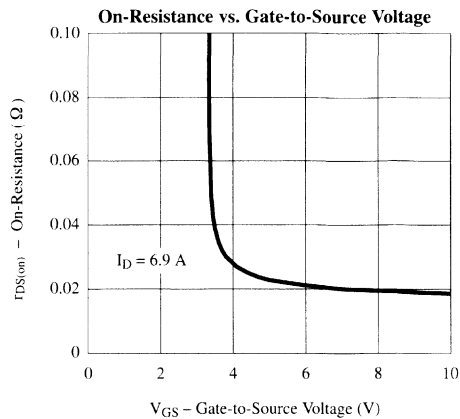
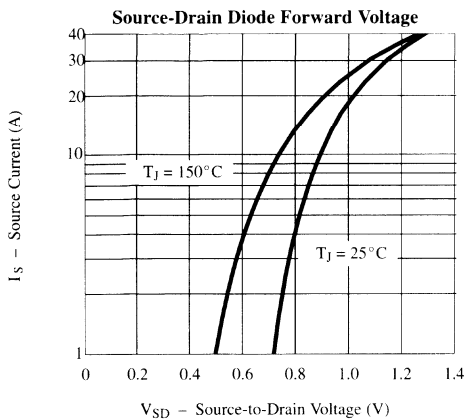
b. Pulse test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Noted)

N-Channel

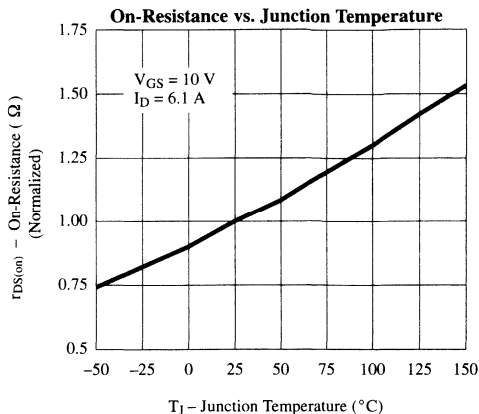
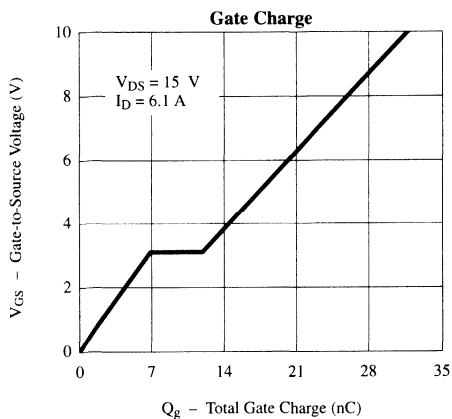
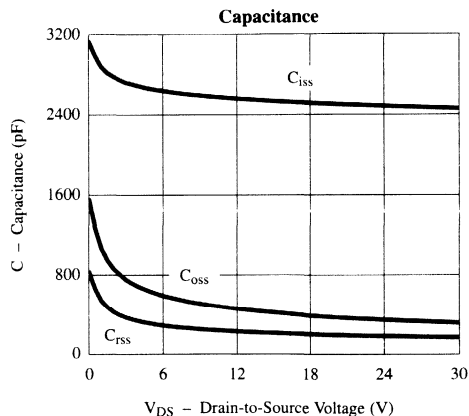
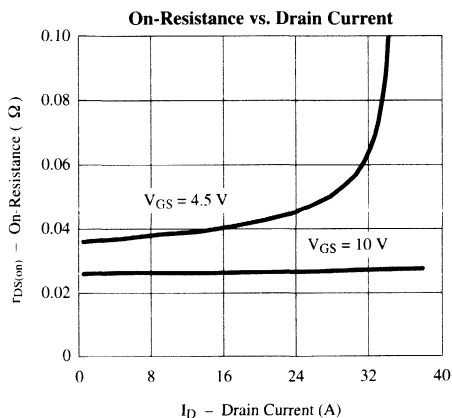
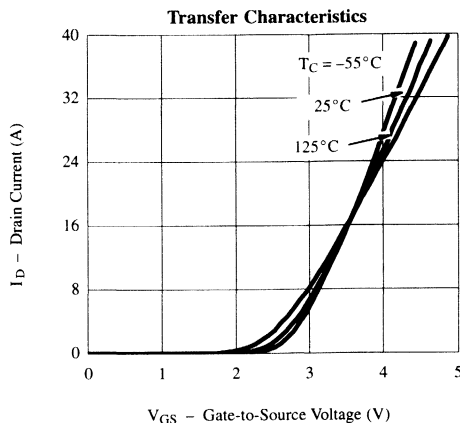
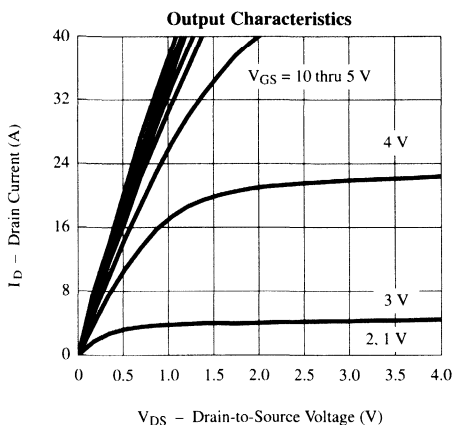


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SOIC-8

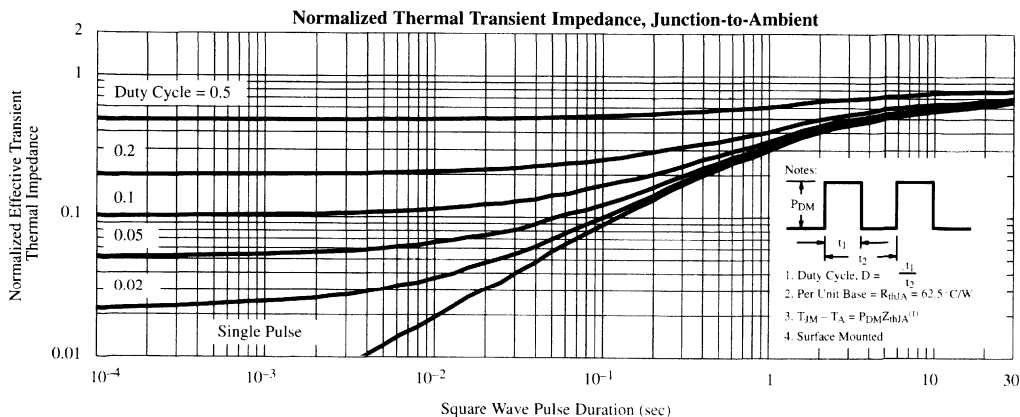
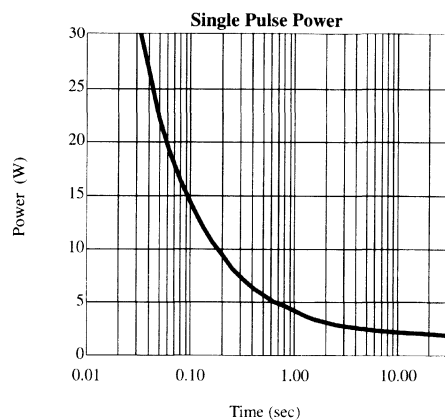
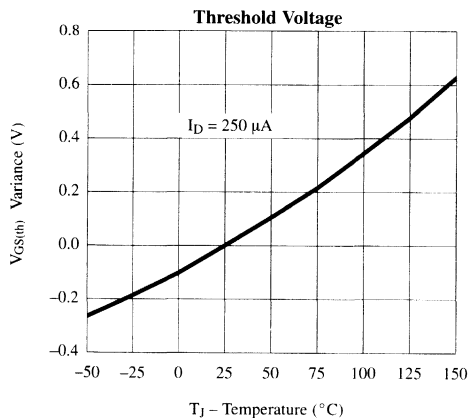
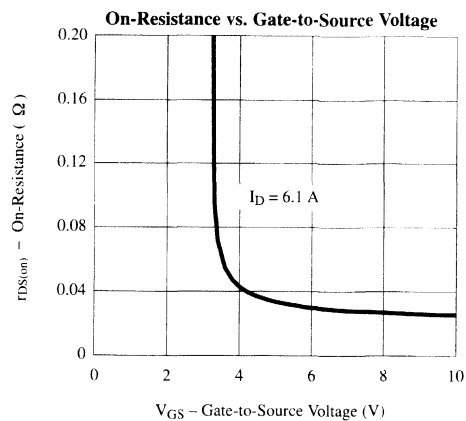
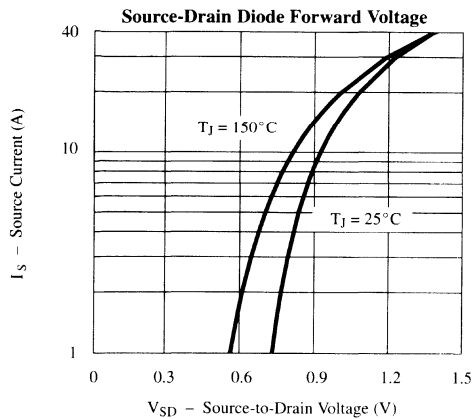
Typical Characteristics (25°C Unless Noted)
N-Channel


Typical Characteristics (25°C Unless Noted)

P-Channel



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SOIC-8

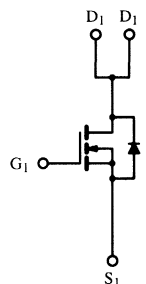
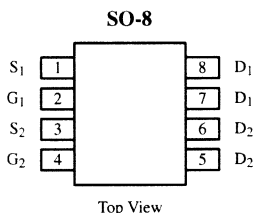
Typical Characteristics (25°C Unless Noted)
P-Channel


Dual N- and P-Channel 60-V, 175°C Rated MOSFET

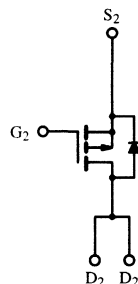
Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	60	0.055 @ V _{GS} = 10 V	± 4.5
		0.075 @ V _{GS} = 4.5 V	± 3.9
P-Channel	-60	0.120 @ V _{GS} = -10 V	± 3.1
		0.150 @ V _{GS} = -4.5 V	± 2.8

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	60	−60	V
Gate-Source Voltage		V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 175 °C) ^a	T _A = 25 °C	I _D	± 4.5	± 3.1	A
	T _A = 70 °C		± 3.8	± 2.6	
Pulsed Drain Current		I _{DM}	± 30	± 30	
Continuous Source Current (Diode Conduction) ^a		I _S	2.0	−2.0	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.4		W
	T _A = 70 °C		1.7		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 175		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70167.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

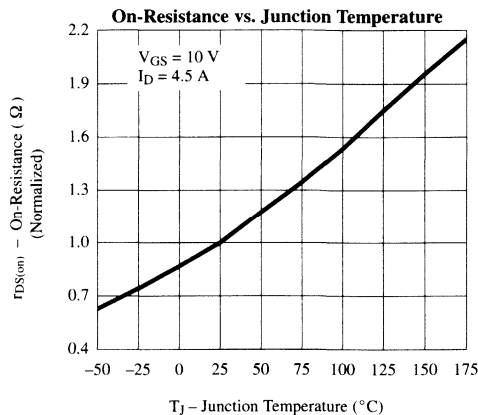
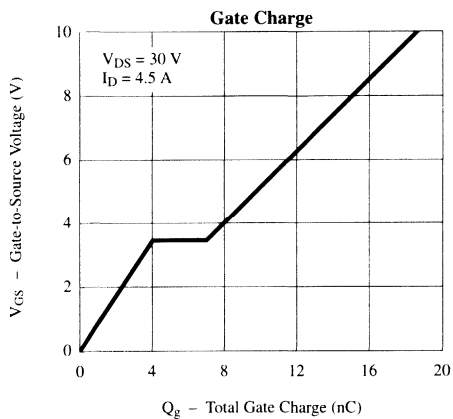
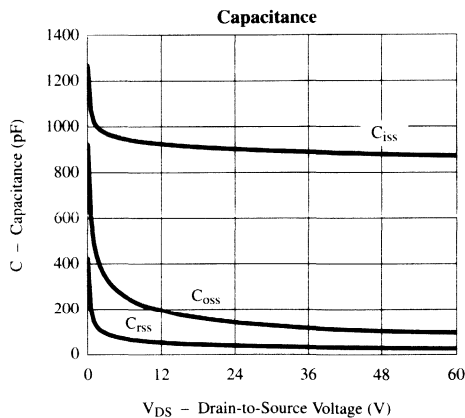
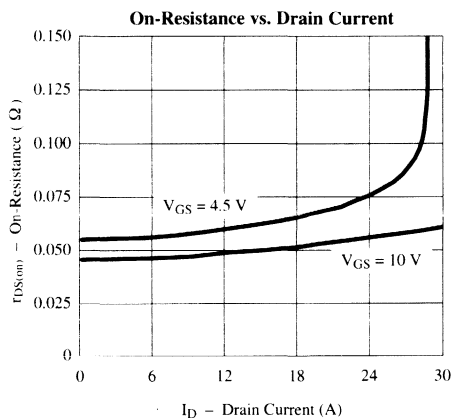
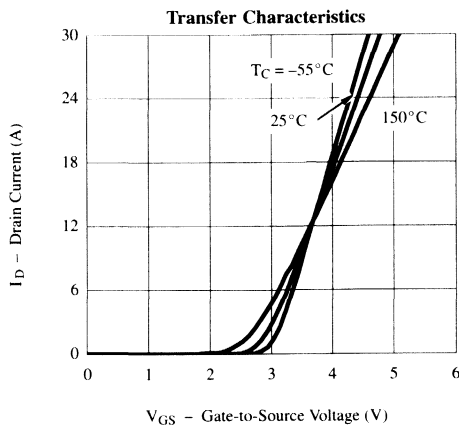
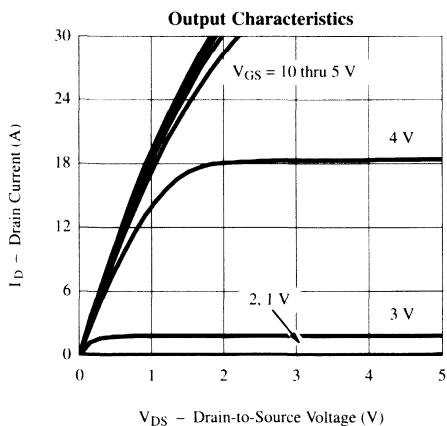
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1		V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	N-Ch		±100	nA	
			P-Ch		±100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	N-Ch		2	μA	
		V _{DS} = -60 V, V _{GS} = 0 V	P-Ch		-2		
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55°C	N-Ch		25		
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 55°C	P-Ch		-25		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	20		A	
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	-20			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.5 A	N-Ch		0.045	Ω	
		V _{GS} = -10 V, I _D = -3.1 A	P-Ch		0.100		
		V _{GS} = 4.5 V, I _D = 3.9 A	N-Ch		0.055		
		V _{GS} = -4.5 V, I _D = -2.8 A	P-Ch		0.125		
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 4.5 A	N-Ch		13	S	
		V _{DS} = -15 V, I _D = -3.1 A	P-Ch		7.5		
Diode Forward Voltage ^b	V _{SD}	I _S = 2.0 A, V _{GS} = 0 V	N-Ch		0.9	V	
		I _S = -2.0 A, V _{GS} = 0 V	P-Ch		-0.8		
Dynamic ^a							
Total Gate Charge	Q _g	N-Channel V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.5 A P-Channel V _{DS} = -30 V, V _{GS} = -10 V I _D = -3.1A	N-Ch		19	30	nC
Gate-Source Charge	Q _{gs}		P-Ch		16	25	
			N-Ch		4		
Gate-Drain Charge	Q _{gd}		P-Ch		4		
		N-Ch		3			
Turn-On Delay Time	t _{d(on)}	P-Ch		1.6			
		N-Ch		13	20		
Rise Time	t _r	P-Ch		8	15		
		N-Ch		11	20		
Turn-Off Delay Time	t _{d(off)}	P-Ch		10	20		
		N-Ch		36	60		
Fall Time	t _f	P-Ch		12	25		
		N-Ch		11	20		
Source-Drain Reverse Recovery Time	t _{rr}	P-Ch		35	50		
		N-Ch		35	60		
		P-Ch		60	90		
		N-Ch					

Notes

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

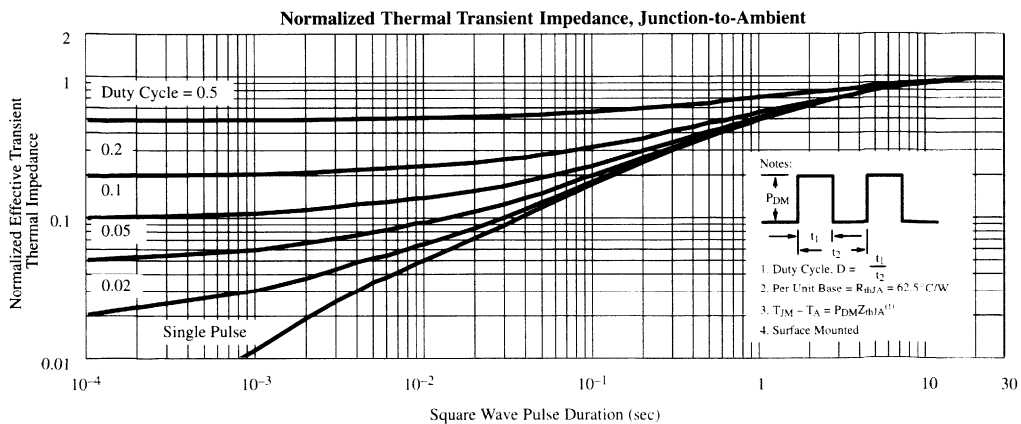
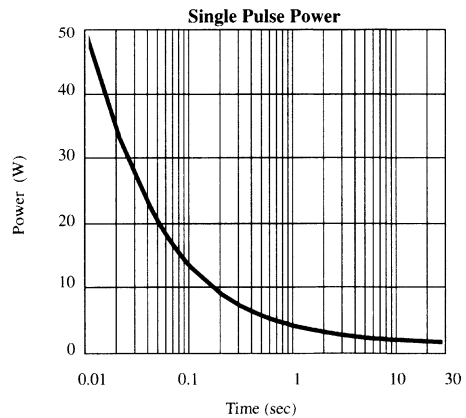
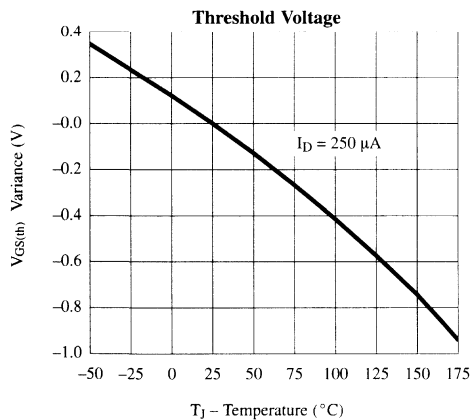
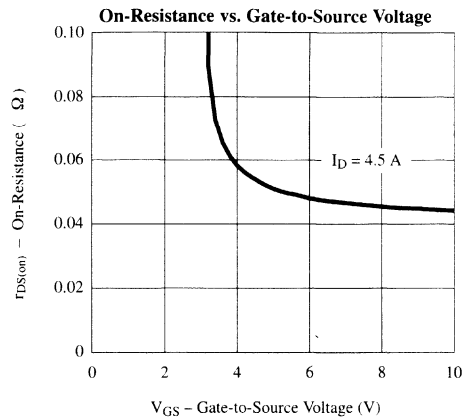
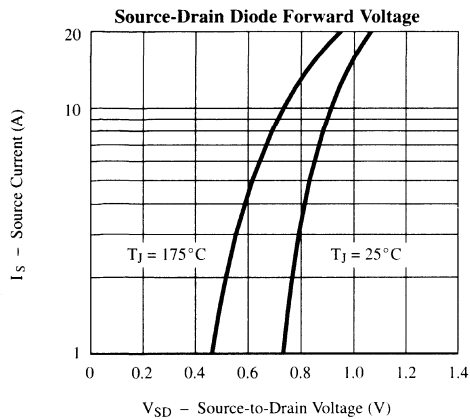
Typical Characteristics (25°C Unless Otherwise Noted) N-Channel



3

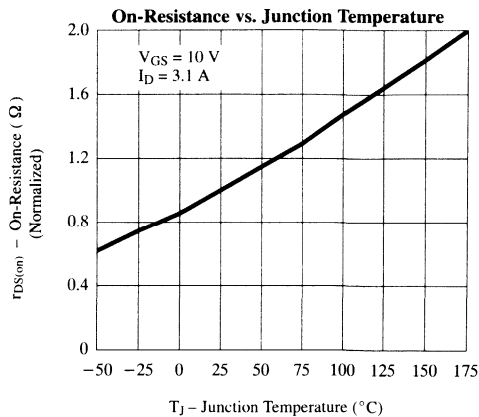
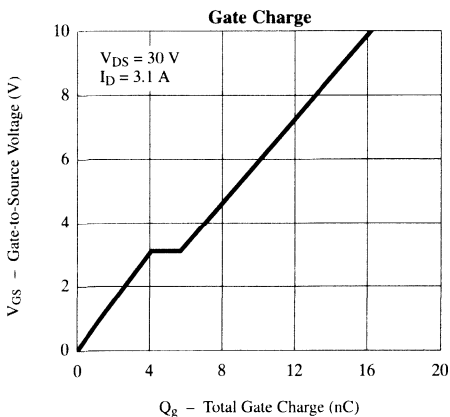
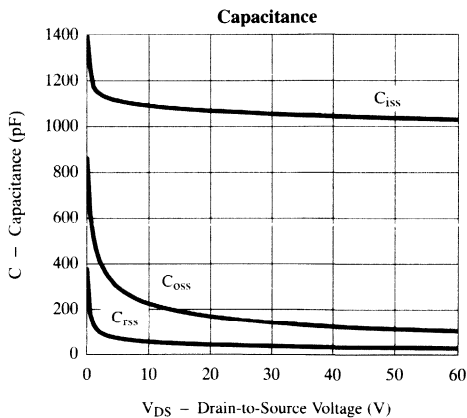
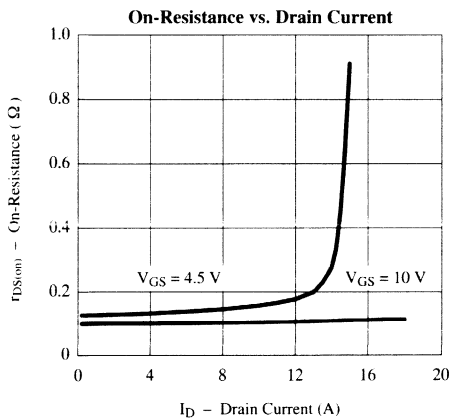
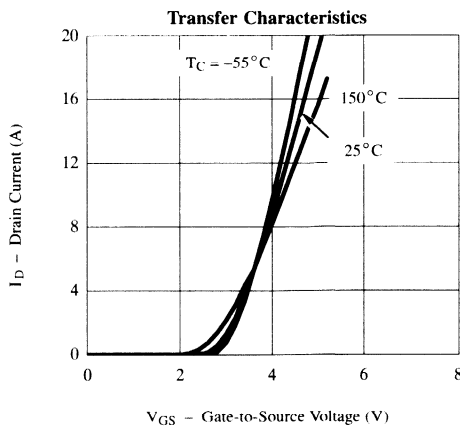
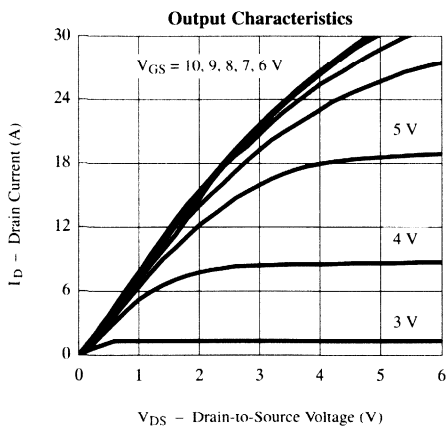
SOIC-8

Typical Characteristics (25°C Unless Otherwise Noted) N-Channel



Typical Characteristics (25°C Unless Noted)

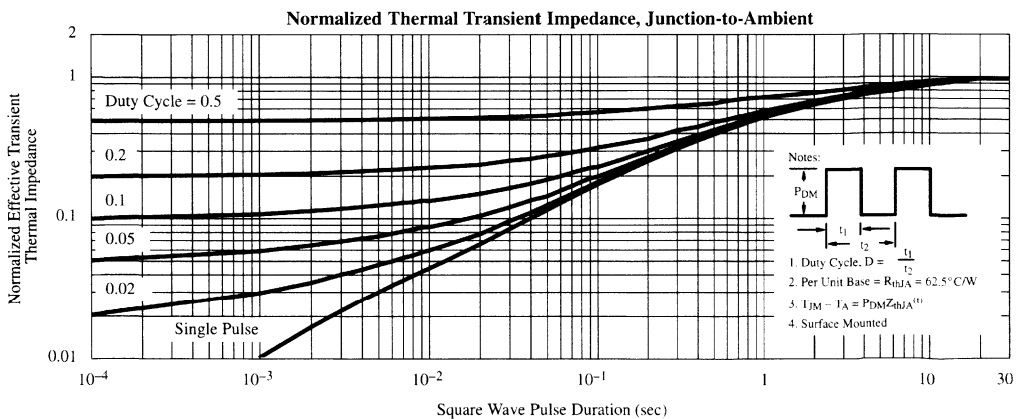
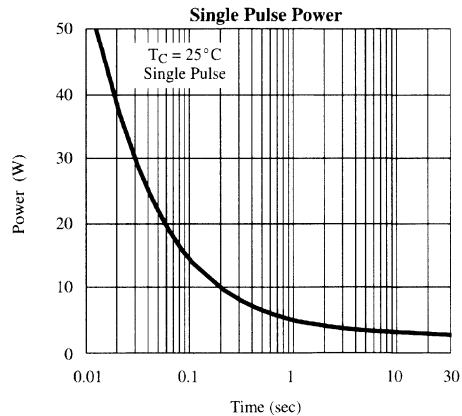
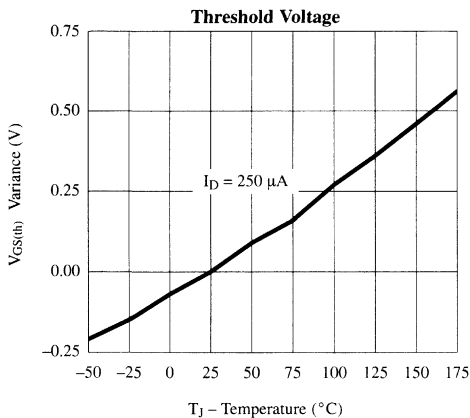
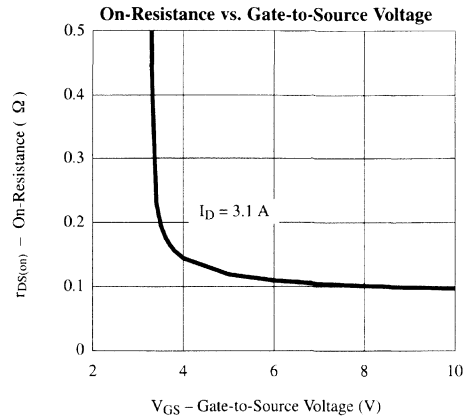
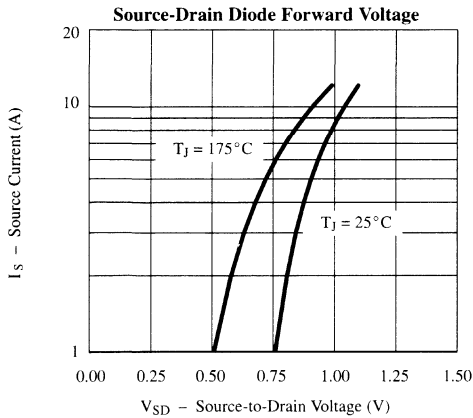
P-Channel



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SOIC-8

Typical Characteristics (25°C Unless Noted)

P-Channel

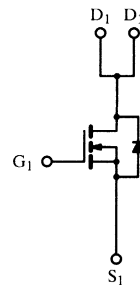
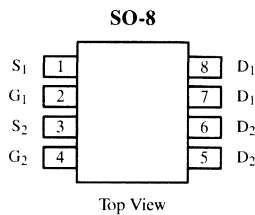


Dual N- and P-Channel 2.5-V (G-S) Rated MOSFET

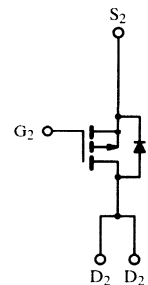
Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.025 @ V _{GS} = 4.5 V	± 7.1
		0.035 @ V _{GS} = 2.5 V	± 6.0
P-Channel	-20	0.033 @ V _{GS} = -4.5 V	± 6.2
		0.050 @ V _{GS} = -2.5 V	± 5.0

TrenchFET™
Power MOSFETs
2.5-V Rated



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	± 12	± 12	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 7.1	± 6.2	A
		± 5.7	± 4.9	
Pulsed Drain Current	I _{DM}	± 40	± 40	
Continuous Source Current (Diode Conduction) ^a	I _S	1.7	-1.7	
Maximum Power Dissipation ^a	P _D	2.0	2.0	W
		1.3	1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^{NO TAG}	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70717.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

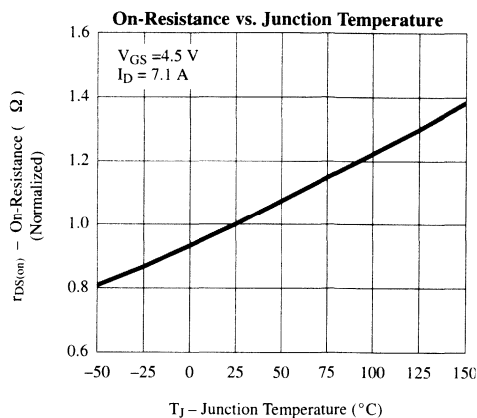
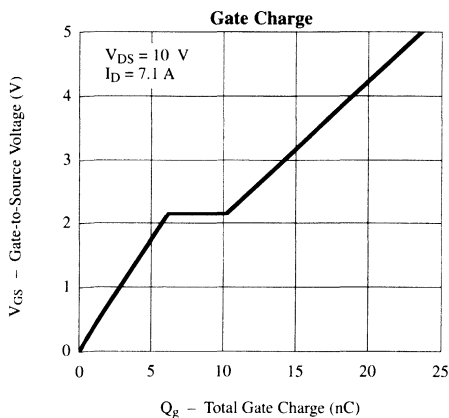
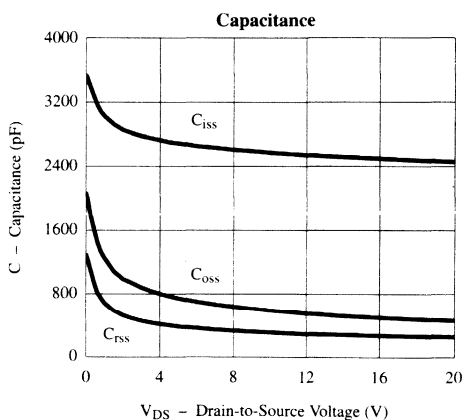
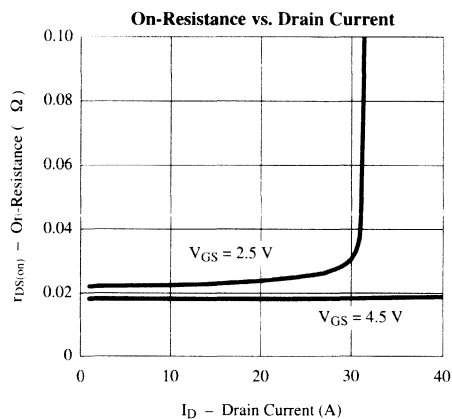
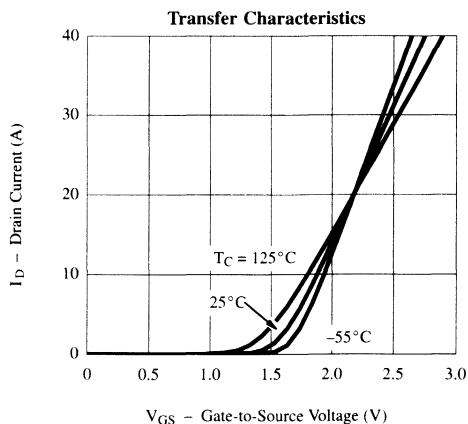
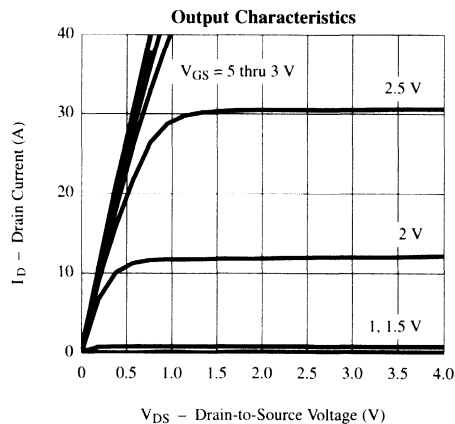
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6		V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.6			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch		± 100	nA	
			P-Ch		± 100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch		-1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55°C	N-Ch		5		
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55°C	P-Ch		-5		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	20		A	
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-20			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 7.1 A	N-Ch		0.019	0.025	Ω
		V _{GS} = -4.5 V, I _D = -6.2 A	P-Ch		0.027	0.033	
		V _{GS} = 2.5 V, I _D = 6.0 A	N-Ch		0.025	0.035	
		V _{GS} = -2.5 V, I _D = -5.0 A	P-Ch		0.040	0.050	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 7.1 A	N-Ch		27		S
		V _{DS} = -10 V, I _D = -6.2 A	P-Ch		20		
Diode Forward Voltage ^b	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch			1.2	V
		I _S = -1.7 A, V _{GS} = 0 V	P-Ch			-1.2	
Dynamic ^{NO TAG}							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 7.1 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -6.2 A	N-Ch		25	50	nC
Gate-Source Charge	Q _{gs}		P-Ch		22	35	
			N-Ch		6.5		
Gate-Drain Charge	Q _{gd}		P-Ch		7		
		N-Ch		4			
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω	P-Ch		3.5		ns
			N-Ch		40	60	
P-Ch			27	50			
N-Ch			40	60			
Rise Time	t _r		P-Ch		32	50	
			N-Ch		90	150	
Turn-Off Delay Time	t _{d(off)}		P-Ch		95	150	
			N-Ch		40	60	
Fall Time	t _f	P-Ch		45	70		
		N-Ch		40	80		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		40	80	
		I _F = -1.7 A, di/dt = 100 A/μs	P-Ch		40	80	

Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Noted)

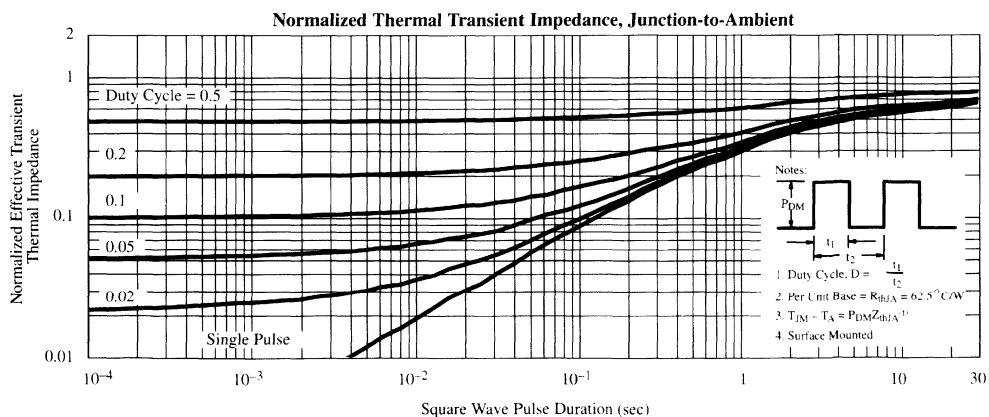
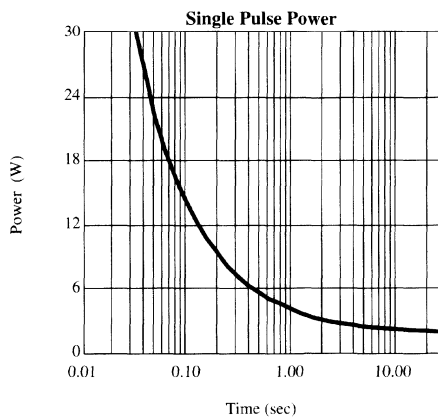
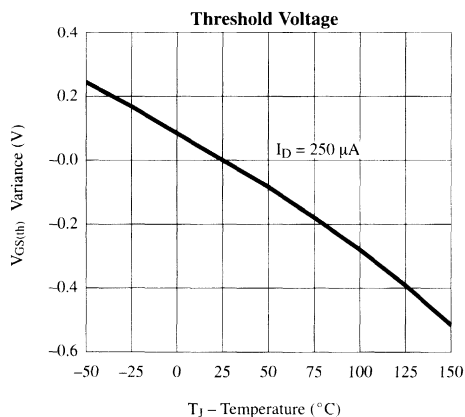
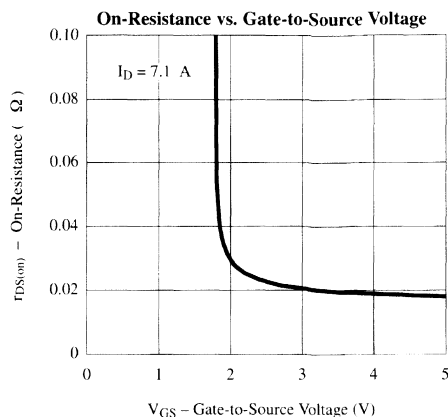
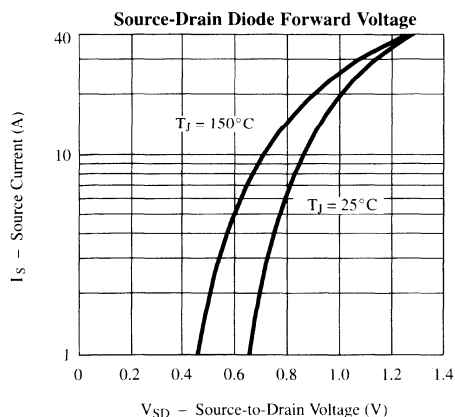
N-Channel



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SOIC-8

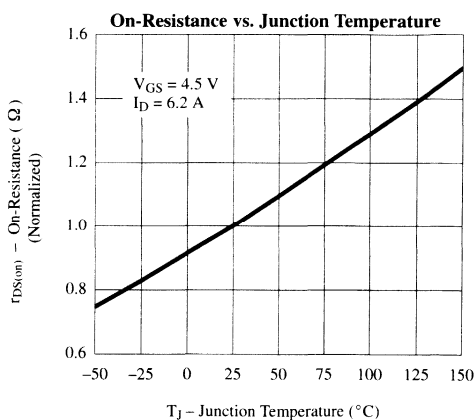
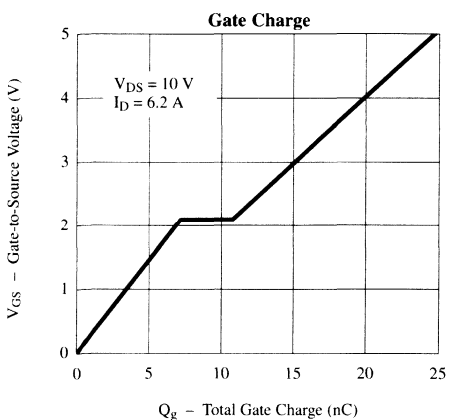
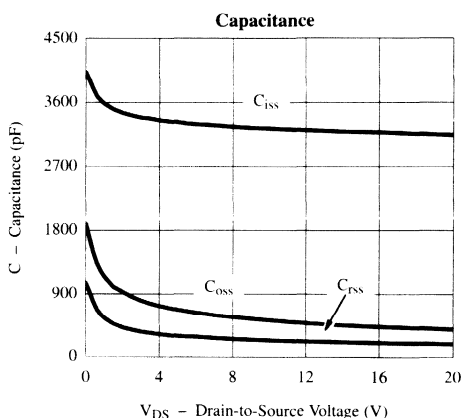
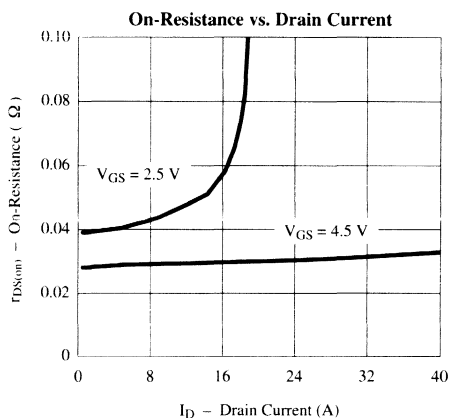
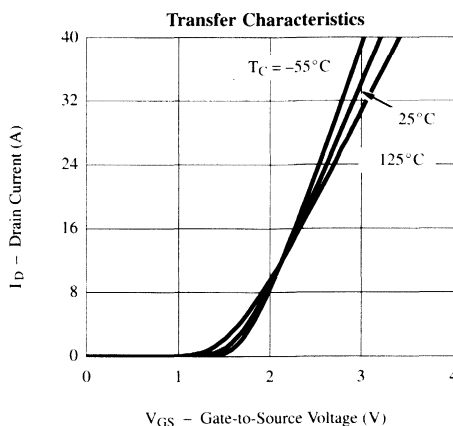
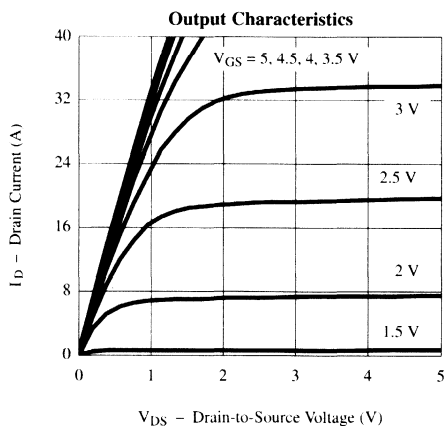
Typical Characteristics (25°C Unless Noted)

N-Channel



Typical Characteristics (25°C Unless Noted)

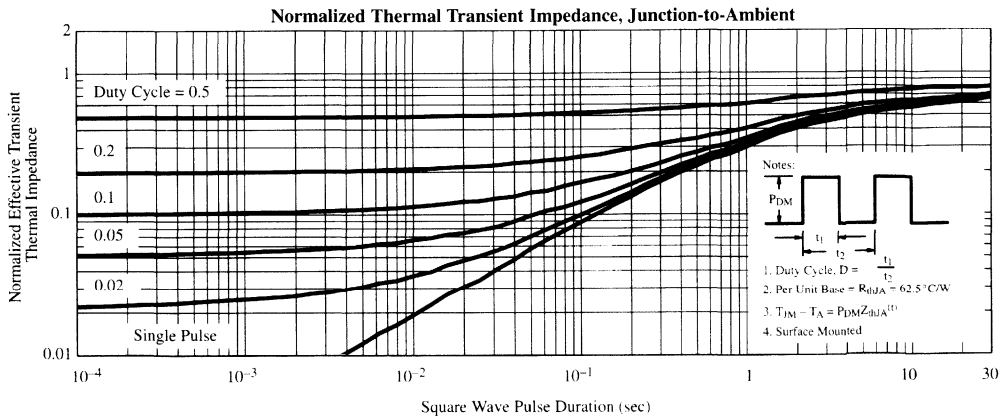
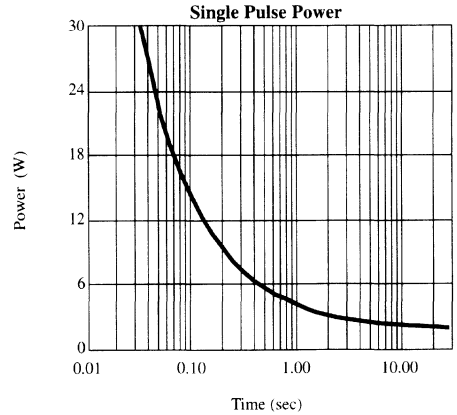
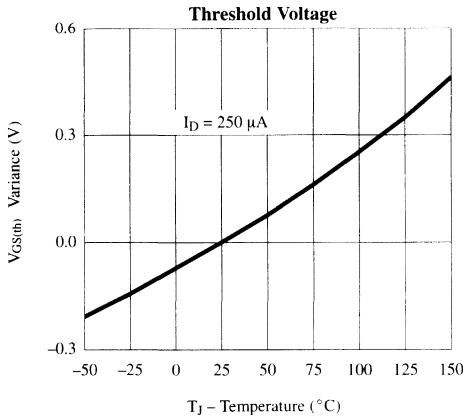
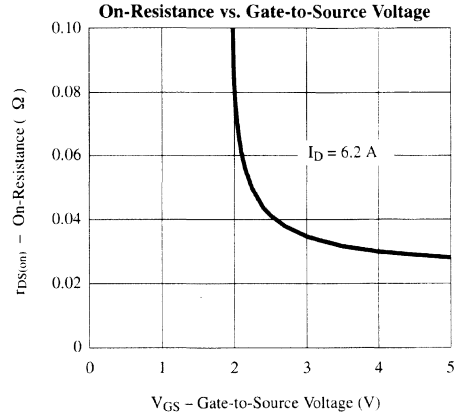
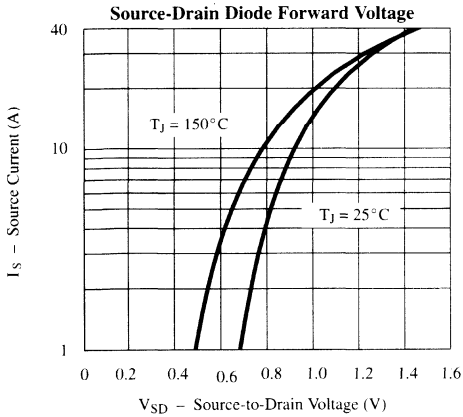
P-Channel



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SOIC-8

Typical Characteristics (25°C Unless Noted)

P-Channel

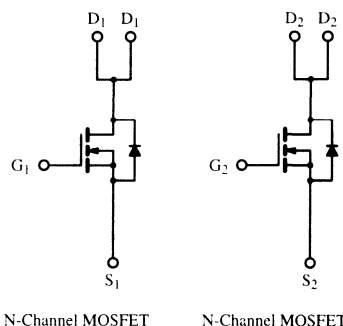
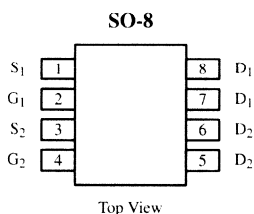


Dual N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.025 @ $V_{GS} = 10$ V	± 6.9
	0.035 @ $V_{GS} = 4.5$ V	± 5.8

TrenchFET™
Power MOSFETs



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70667.

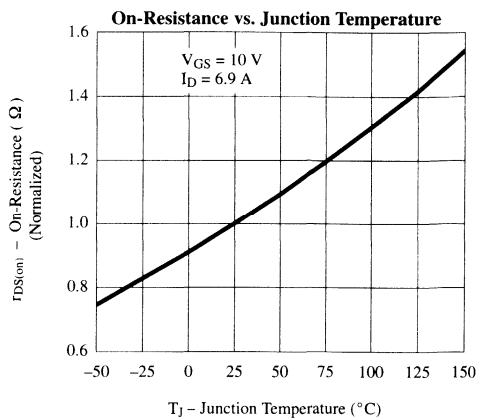
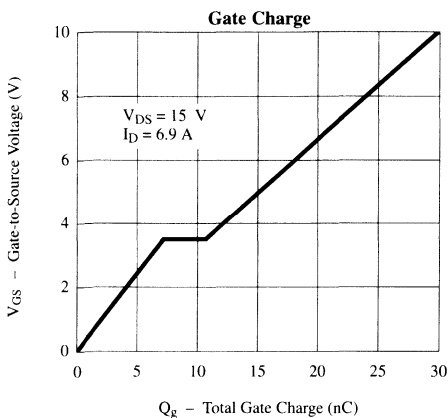
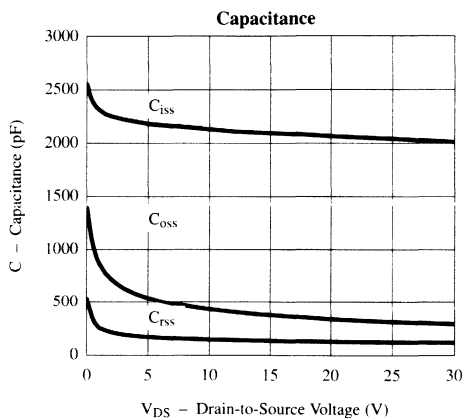
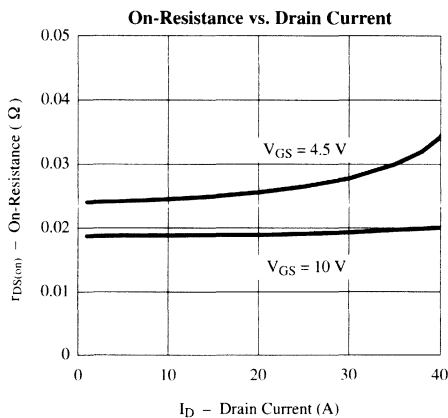
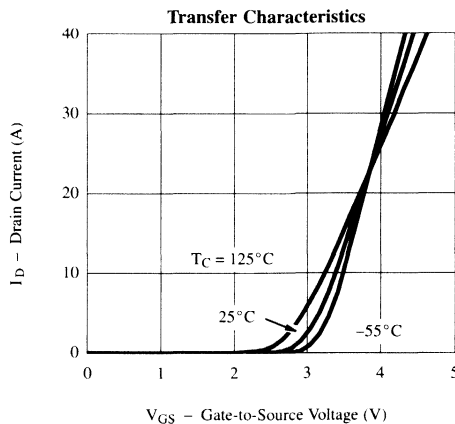
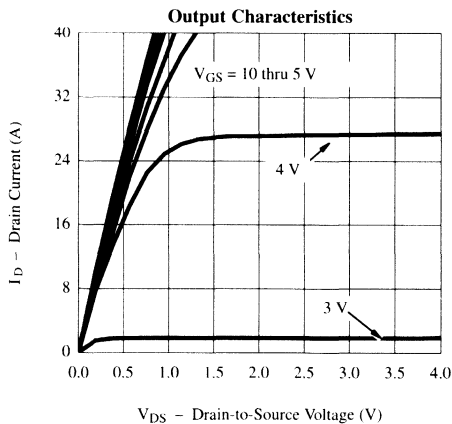
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 6.9\ \text{A}$		0.020	0.025	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 5.8\ \text{A}$		0.026	0.035	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 6.9\ \text{A}$		25		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 6.9\ \text{A}$		30	50	nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		12	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			60	90	
Fall Time	t_f			15	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	90	

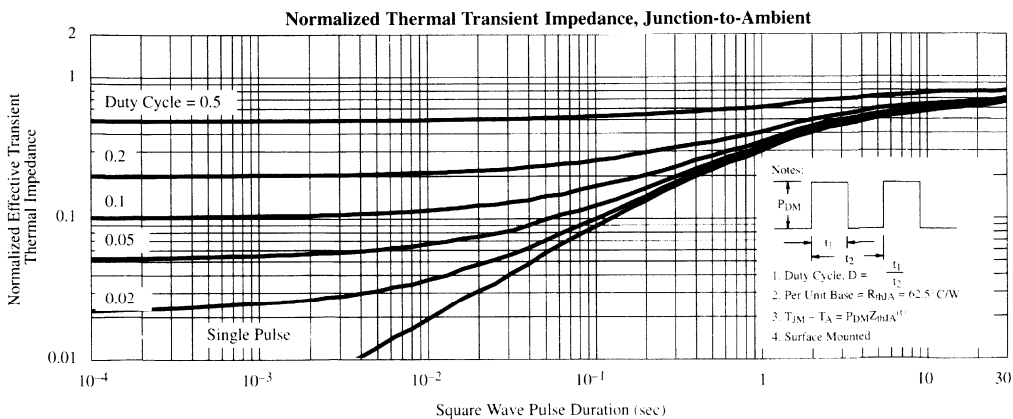
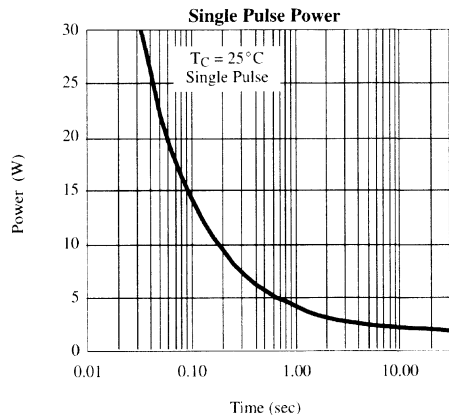
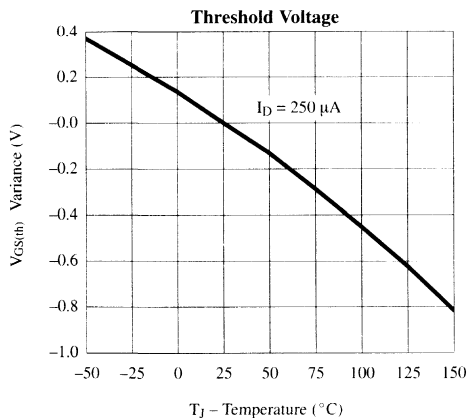
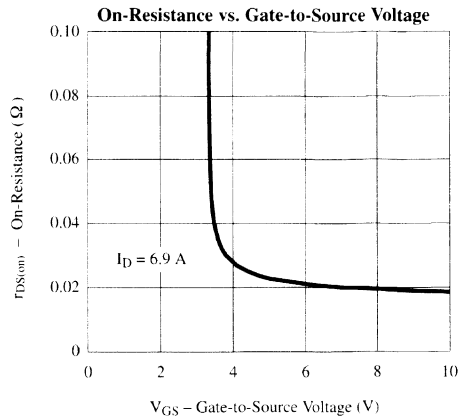
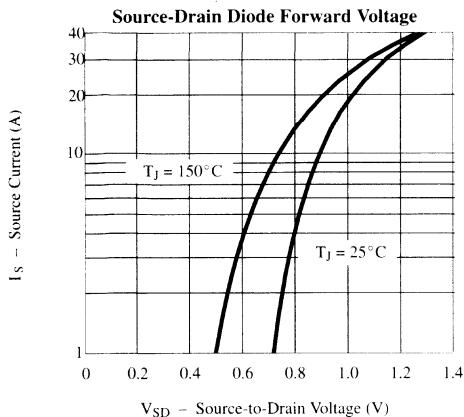
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)



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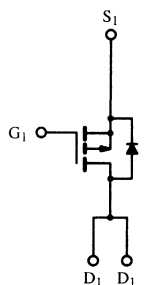
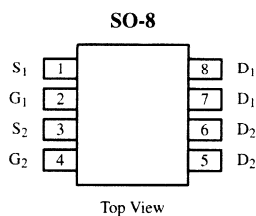
Typical Characteristics (25°C Unless Otherwise Noted)


Dual P-Channel 30-V (D-S) Rated MOSFET

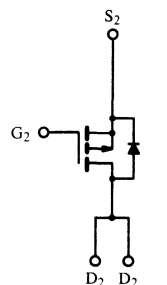
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.032 @ $V_{GS} = -10$ V	± 6.1
	0.045 @ $V_{GS} = -4.5$ V	± 5.1

TrenchFET™
Power MOSFETs



P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 6.1	A
		± 4.9	
Pulsed Drain Current	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	
Maximum Power Dissipation ^a	P_D	2.0	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70642. A SPICE Model data sheet is available for this product (FaxBack document #70635).

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

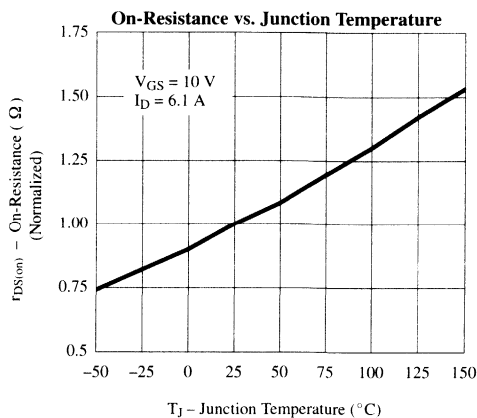
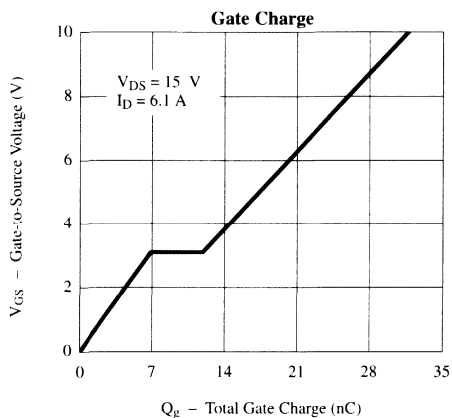
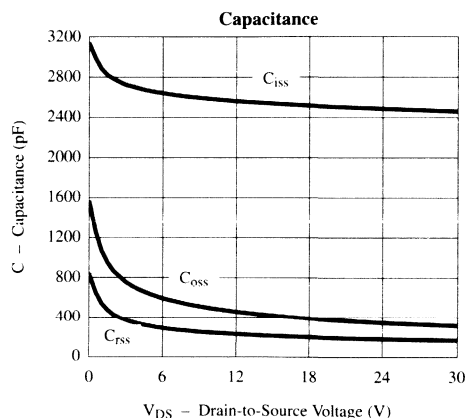
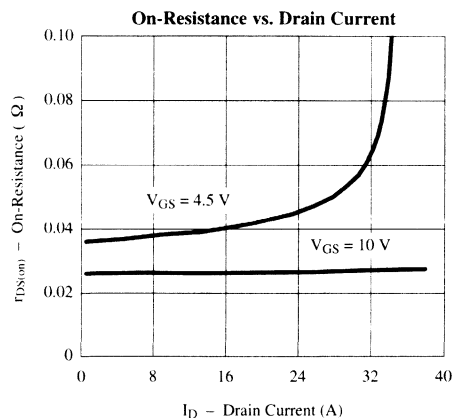
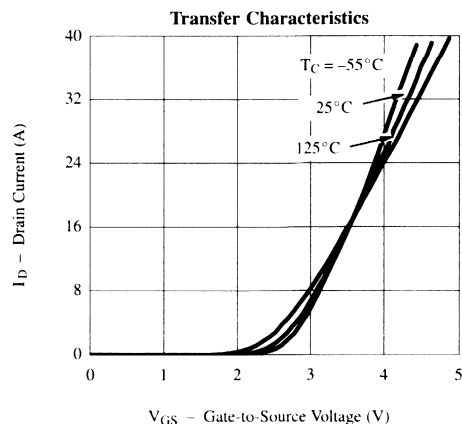
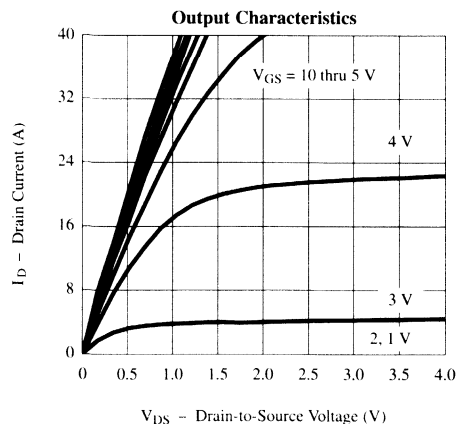
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -10\ \text{V}$	-20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}$, $I_D = -6.1\ \text{A}$		0.026	0.032	Ω
		$V_{GS} = -4.5\ \text{V}$, $I_D = -5.1\ \text{A}$		0.036	0.045	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -6.1\ \text{A}$		16		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -1.7\ \text{A}$, $V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}$, $V_{GS} = -10\ \text{V}$, $I_D = -6.1\ \text{A}$		32.0	50	nC
Gate-Source Charge	Q_{gs}			7.0		
Gate-Drain Charge	Q_{gd}			5.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \equiv -1\ \text{A}$, $V_{GEN} = -10\ \text{V}$, $R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			55	80	
Fall Time	t_f			25	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		50	90	

Notes

a. For design aid only; not subject to production testing.

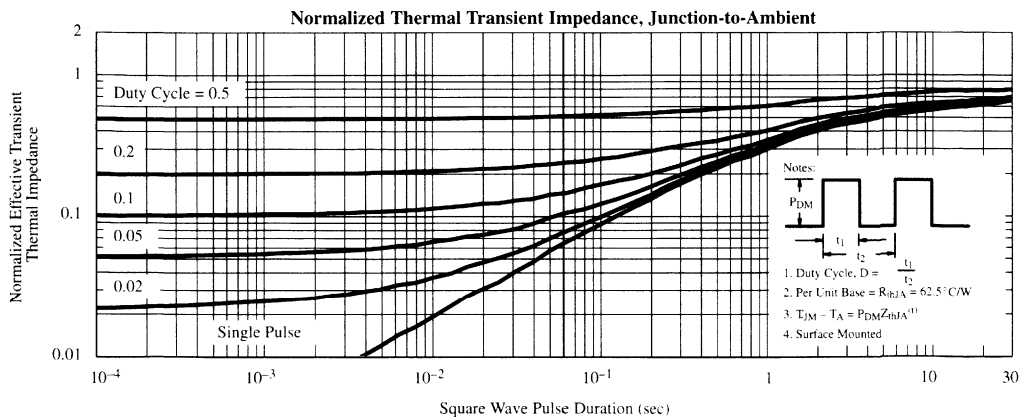
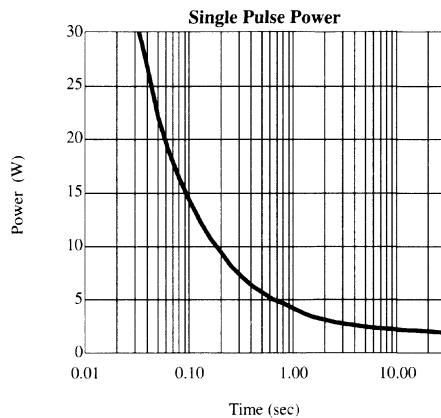
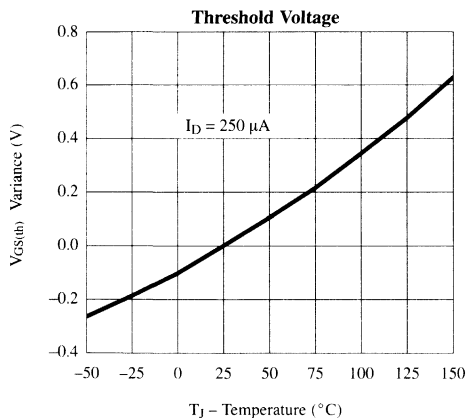
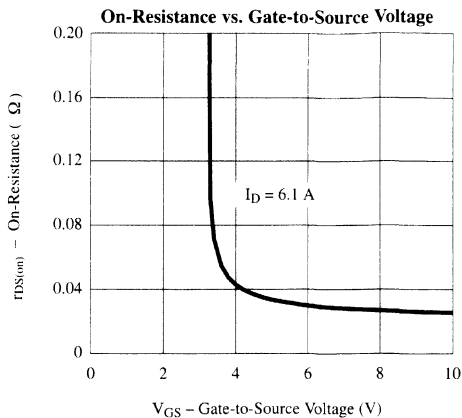
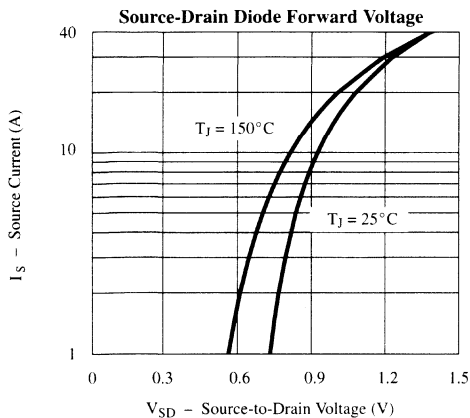
b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Noted)



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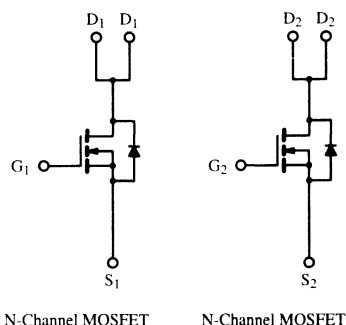
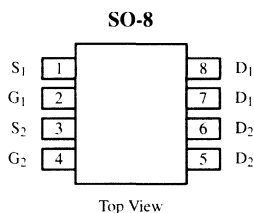
Typical Characteristics (25°C Unless Noted)



Dual N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.037 @ $V_{GS} = 10$ V	± 5.8
	0.055 @ $V_{GS} = 4.5$ V	± 4.7



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 5.8	A
	$T_A = 70^\circ\text{C}$		± 4.6	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a		I_S	1.7	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70150. A SPICE Model data sheet is available for this product (FaxBack document #70556).

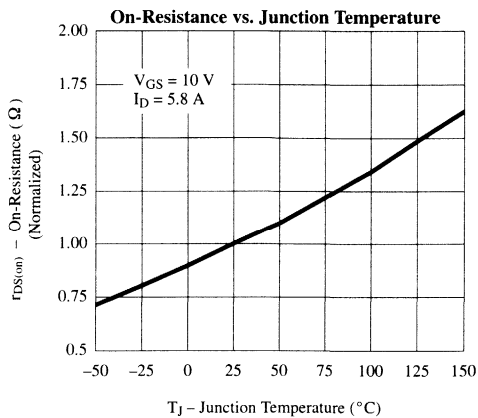
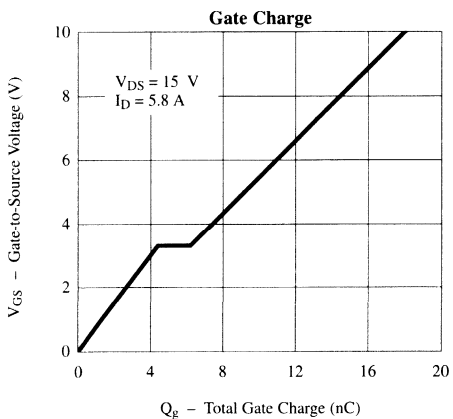
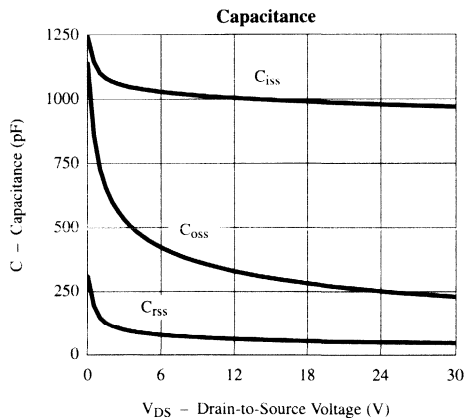
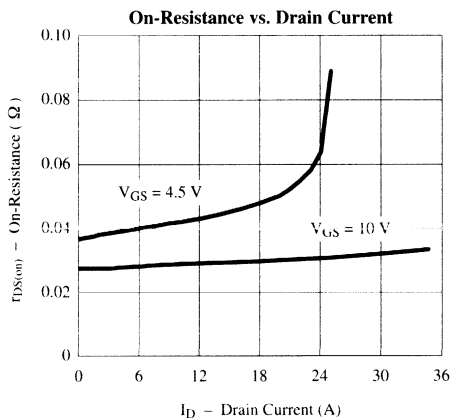
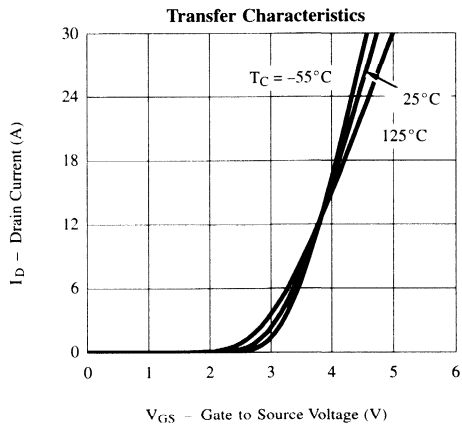
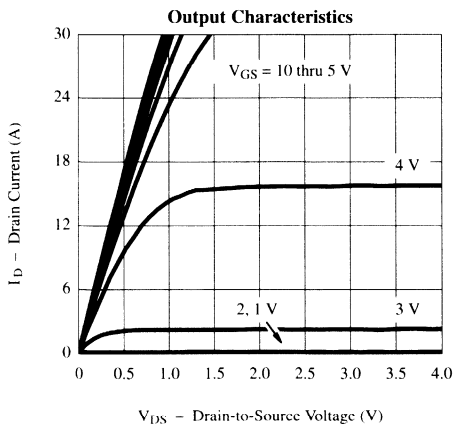
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

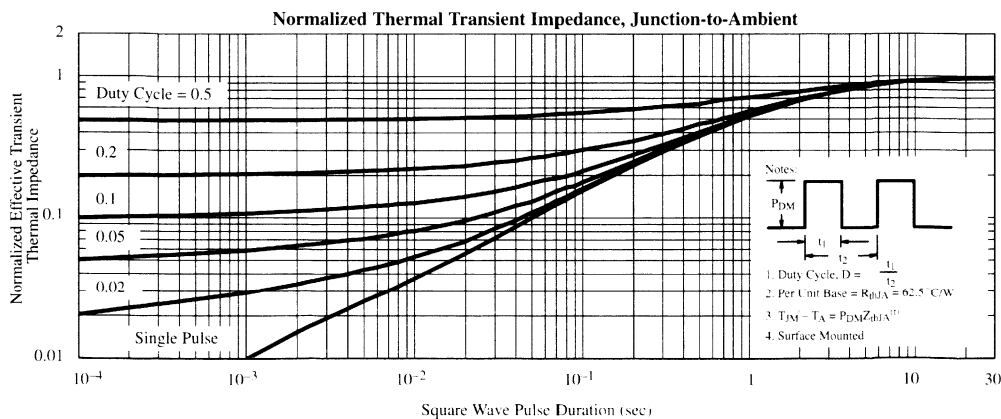
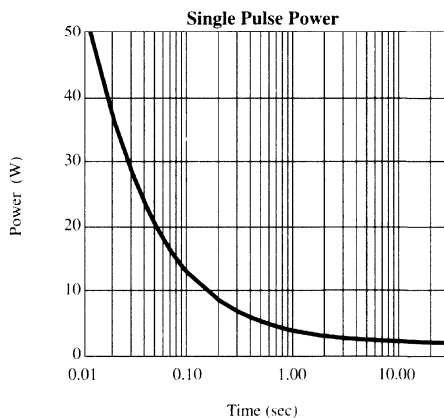
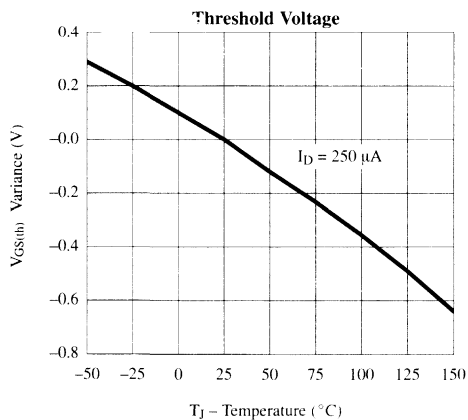
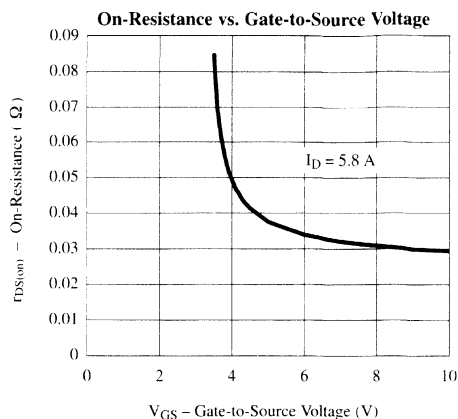
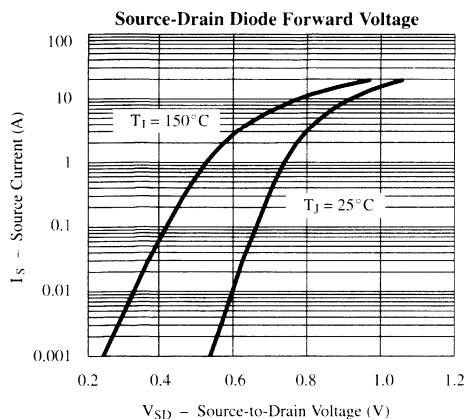
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 5.8\ \text{A}$		0.030	0.037	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 4.7\ \text{A}$		0.042	0.055	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 5.8\ \text{A}$		13		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 5.8\ \text{A}$		18	25	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			2.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		10	16	ns
Rise Time	t_r			10	16	
Turn-Off Delay Time	$t_{d(off)}$			27	40	
Fall Time	t_f			24	35	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		45	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



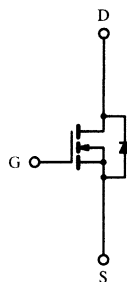
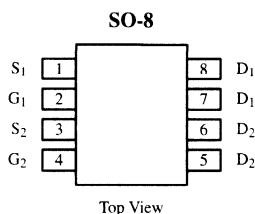
Typical Characteristics (25°C Unless Otherwise Noted)


Dual N-Channel 60-V, 175°C Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.055 @ $V_{GS} = 10$ V	± 4.5
	0.075 @ $V_{GS} = 4.5$ V	± 3.9

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$ ± 4.5	A
		$T_A = 70^\circ\text{C}$ ± 3.8	
Pulsed Drain Current	I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I_S	2	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$ 2.4	W
		$T_A = 70^\circ\text{C}$ 1.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

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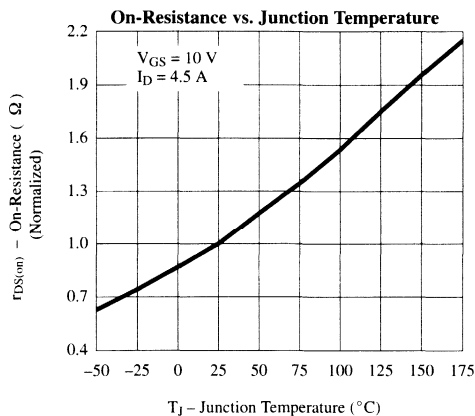
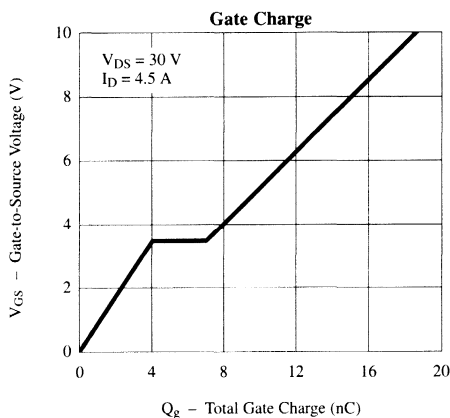
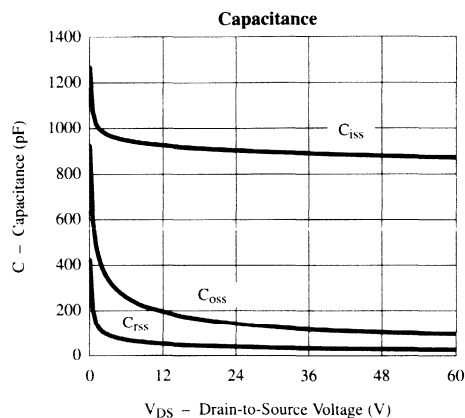
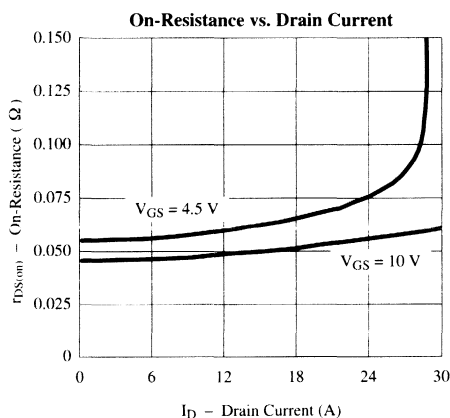
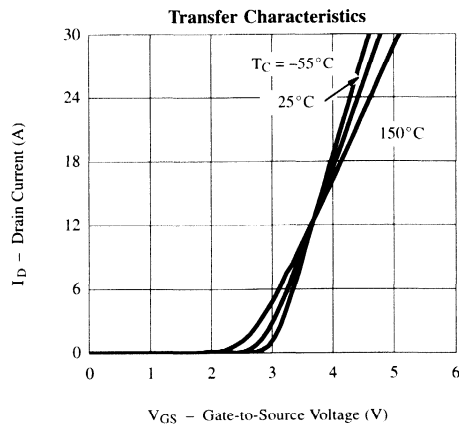
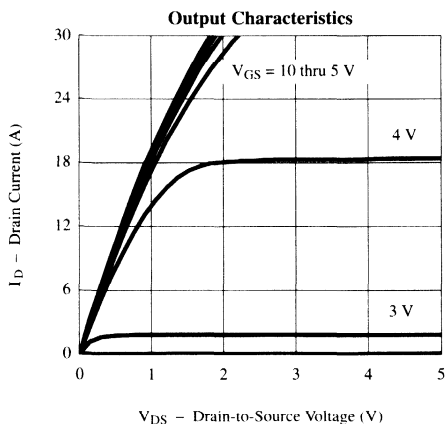
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

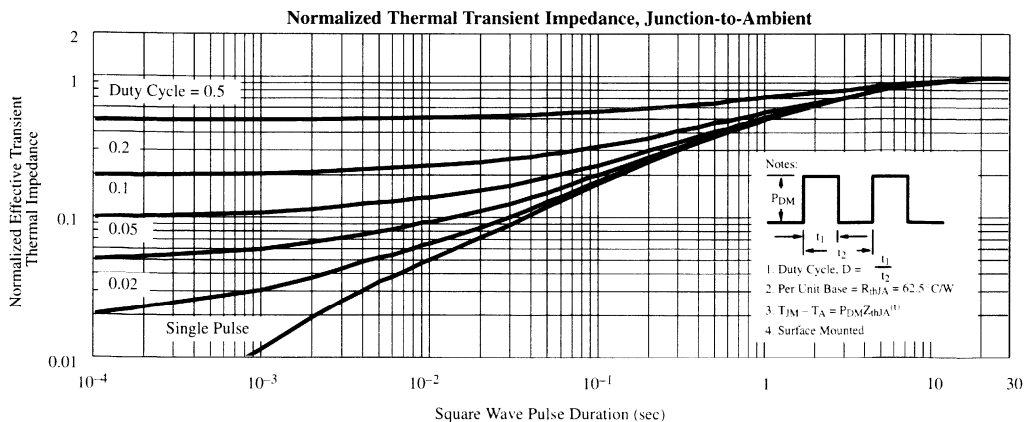
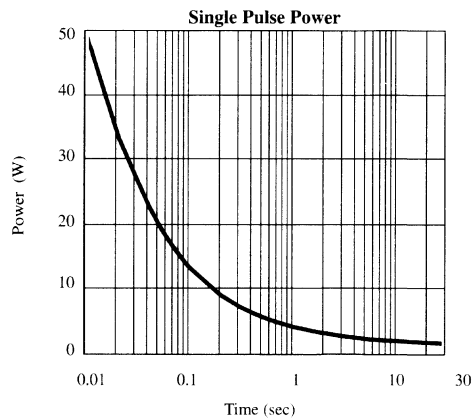
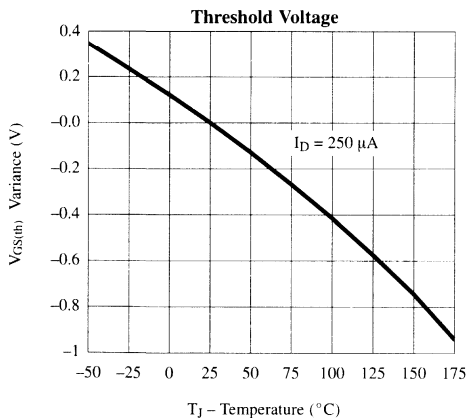
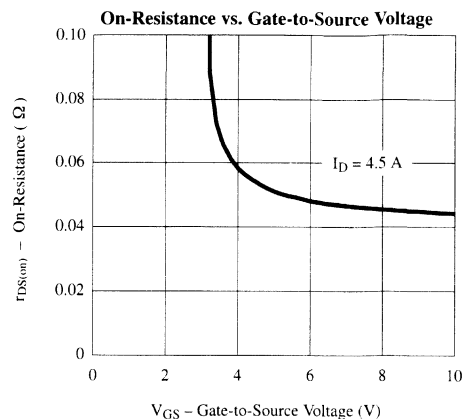
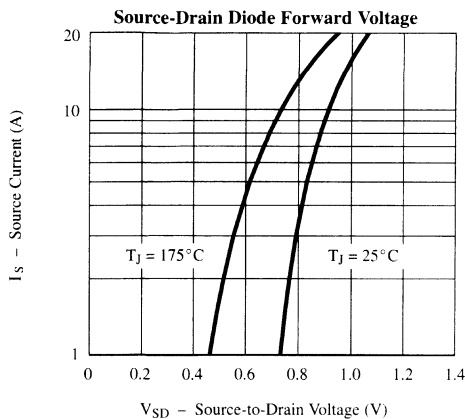
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$			2	μA
		$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 4.5\ \text{A}$		0.045	0.055	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 3.9\ \text{A}$		0.055	0.075	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 4.5\ \text{A}$		13		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.9	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 30\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 4.5\ \text{A}$		19	30	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\ \text{V}$, $R_L = 30\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		13	20	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			36	60	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		35	60	

Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



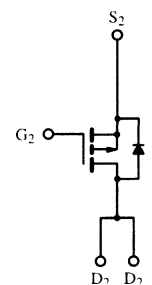
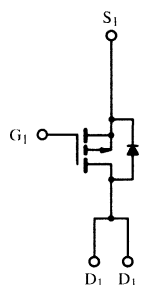
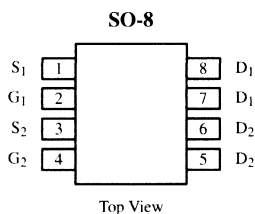
Typical Characteristics (25°C Unless Otherwise Noted)


Dual P-Channel 60-V, 175°C Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-60	0.120 @ V _{GS} = -10 V	± 3.1
	0.150 @ V _{GS} = -4.5 V	± 2.8

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 175°C) ^a	I _D	± 3.1	A
		± 2.6	
Pulsed Drain Current	I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I _S	-2.0	
Maximum Power Dissipation ^a	P _D	2.4	W
		1.7	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

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Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

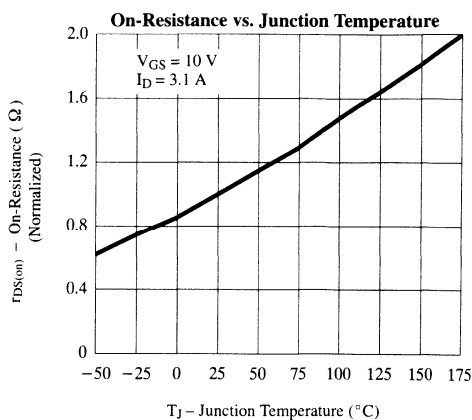
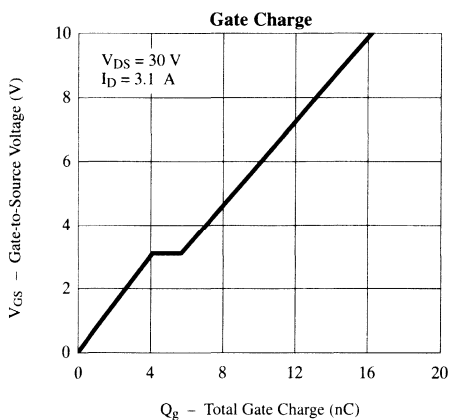
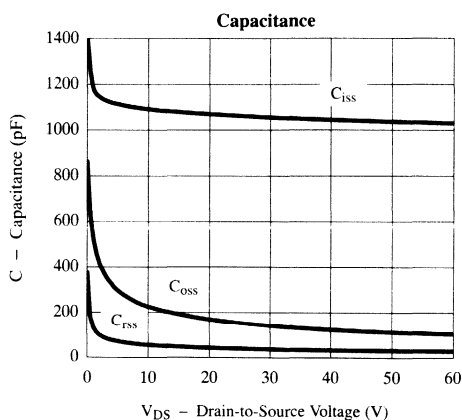
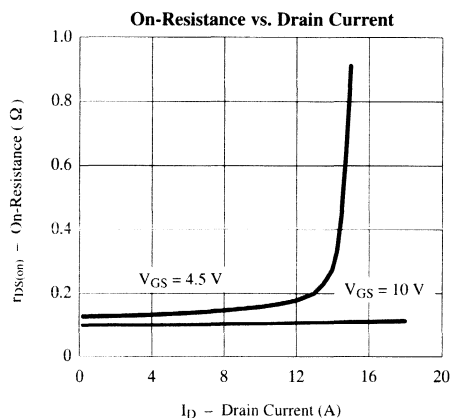
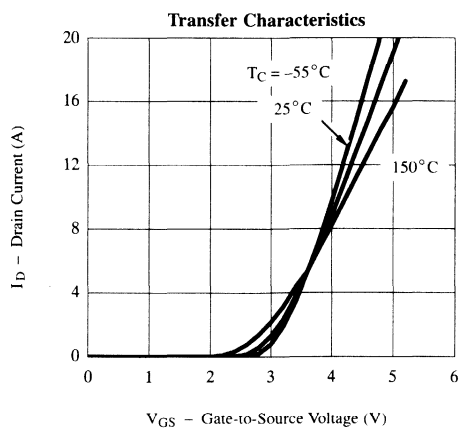
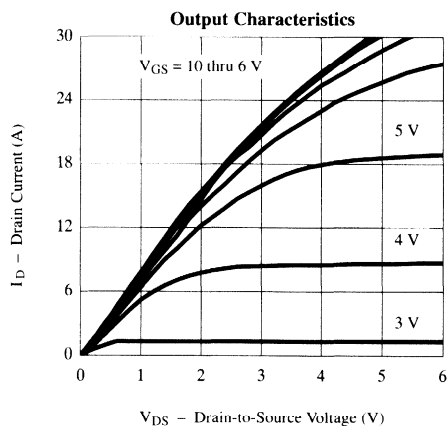
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\ \text{V}$, $V_{GS} = 0\ \text{V}$			-2	μA
		$V_{DS} = -60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -10\ \text{V}$	-20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}$, $I_D = -3.1\ \text{A}$		0.100	0.120	Ω
		$V_{GS} = -4.5\ \text{V}$, $I_D = -2.8\ \text{A}$		0.125	0.150	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -3.1\ \text{A}$		7.5		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.0\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -30\ \text{V}$, $V_{GS} = -10\ \text{V}$, $I_D = -3.1\ \text{A}$		16	25	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\ \text{V}$, $R_L = 30\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -10\ \text{V}$, $R_G = 6\ \Omega$		8	15	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			12	25	
Fall Time	t_f			35	50	
Source-Drain Reverse Recovery Time	t_{rr}			60	90	

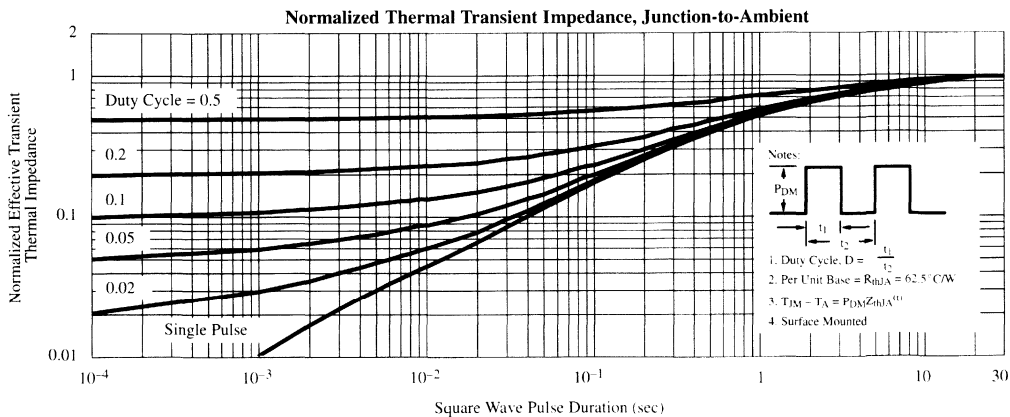
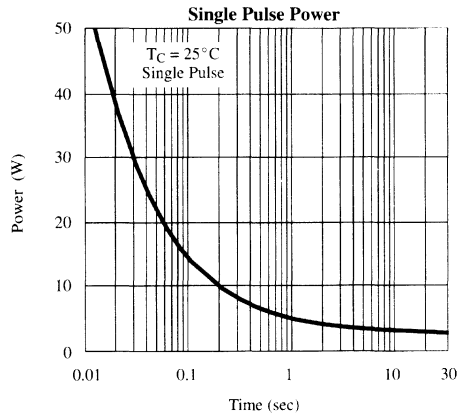
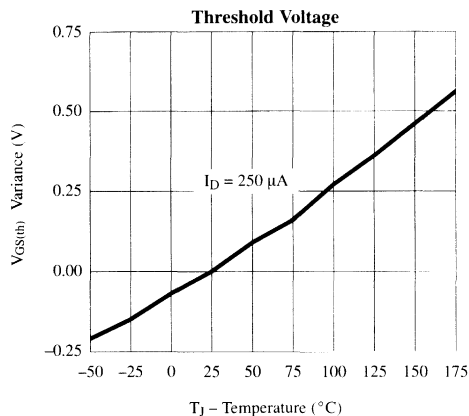
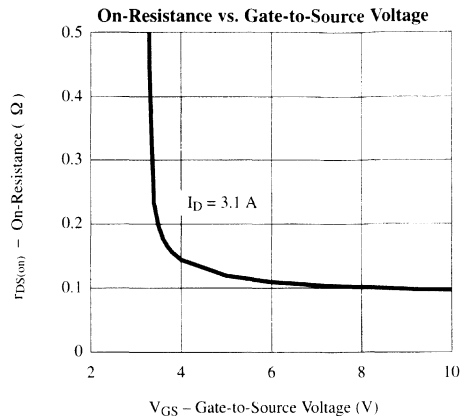
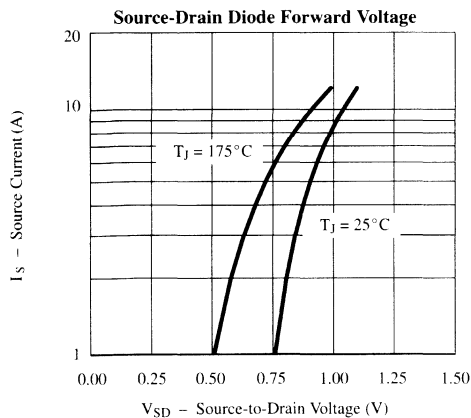
Notes

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Noted)



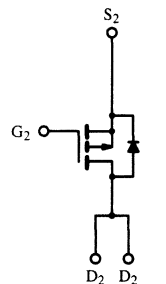
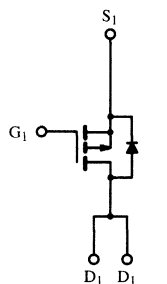
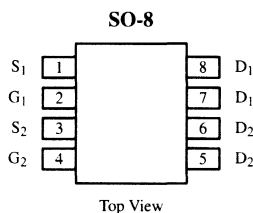
Typical Characteristics (25°C Unless Noted)


Dual P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.033 @ $V_{GS} = -4.5$ V	± 6.2
	0.050 @ $V_{GS} = -2.5$ V	± 5

TrenchFET™
Power MOSFETs
2.5-V Rated



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 6.2	A
		± 4.9	
Pulsed Drain Current	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	
Maximum Power Dissipation ^a	P_D	2.0	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70665.

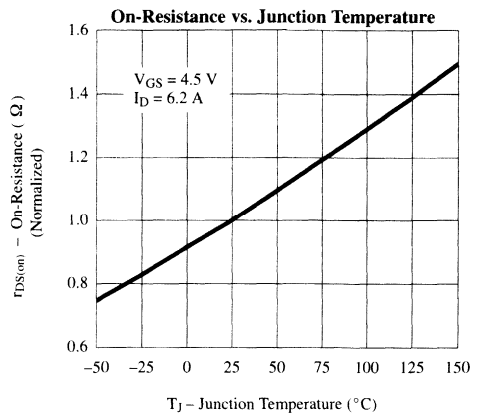
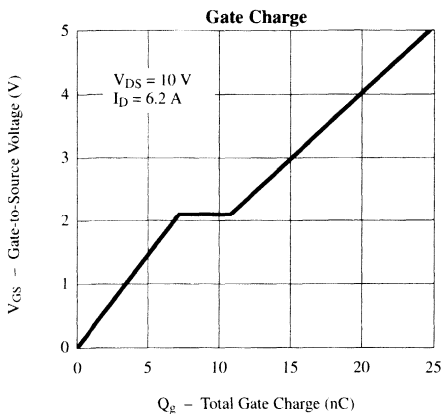
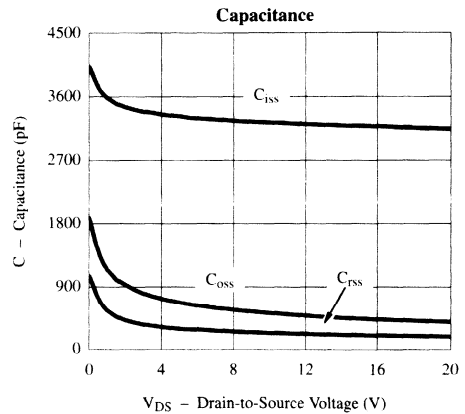
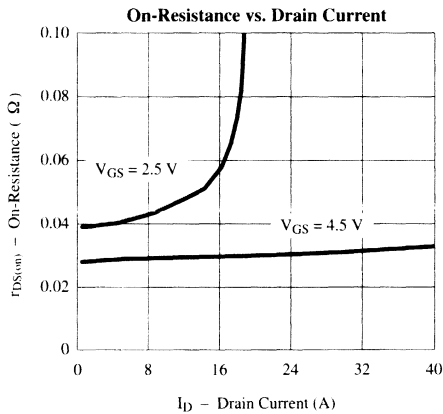
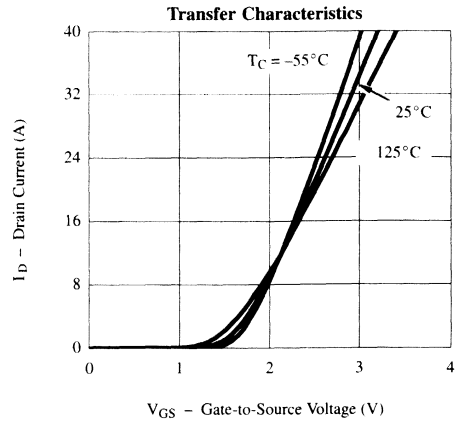
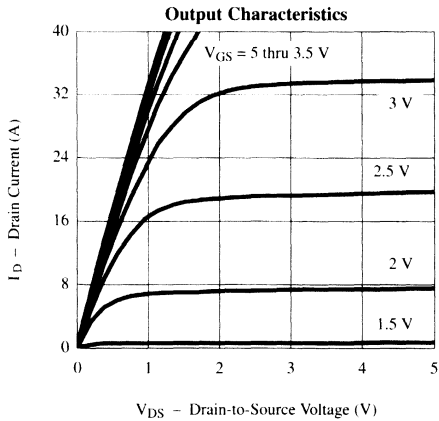
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -4.5\ \text{V}$	-20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}$, $I_D = -6.2\ \text{A}$		0.027	0.033	Ω
		$V_{GS} = -2.5\ \text{V}$, $I_D = -5\ \text{A}$		0.04	0.050	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -10\ \text{V}$, $I_D = -6.2\ \text{A}$		20		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -1.7\ \text{A}$, $V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}$, $V_{GS} = -4.5\ \text{V}$, $I_D = -6.2\ \text{A}$		22	35	nC
Gate-Source Charge	Q_{gs}			7		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -10\ \text{V}$, $R_G = 6\ \Omega$		27	50	ns
Rise Time	t_r			32	50	
Turn-Off Delay Time	$t_{d(off)}$			95	150	
Fall Time	t_f			45	70	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		40	80	

Notes

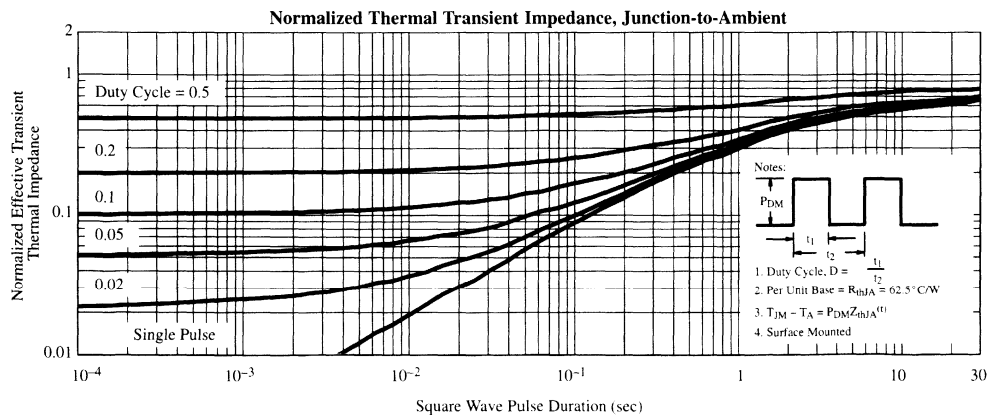
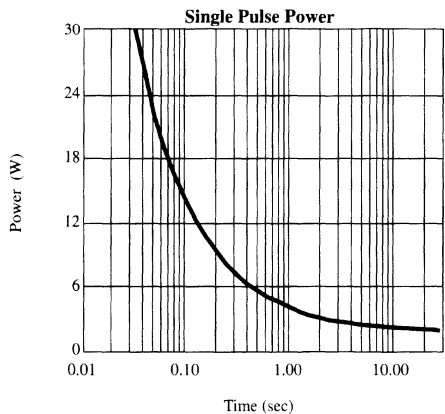
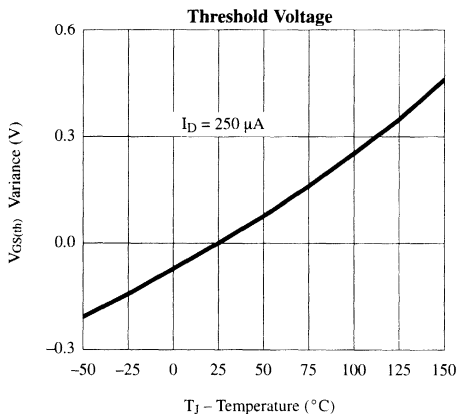
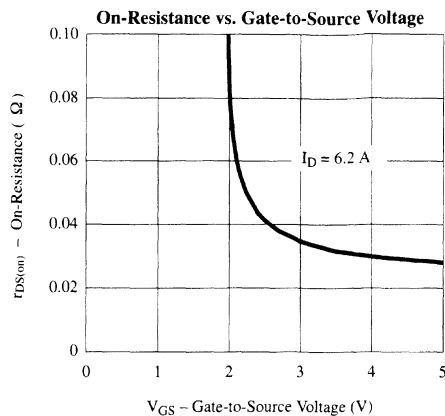
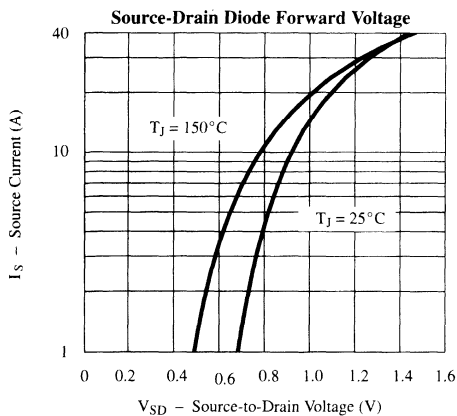
- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Noted)



3
SOIC-8

Typical Characteristics (25°C Unless Noted)

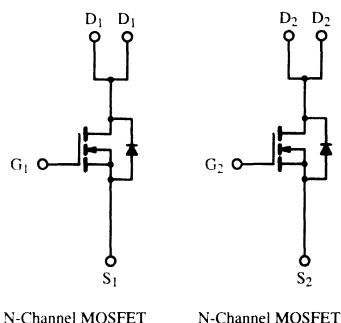
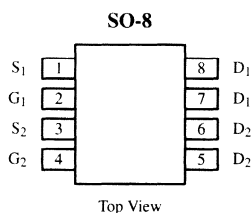


Dual N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.025 @ $V_{GS} = 4.5$ V	± 7.1
	0.035 @ $V_{GS} = 2.5$ V	± 6.0

TrenchFET™
Power MOSFETs
2.5-V Rated



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 7.1	A
		± 5.7	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	
Maximum Power Dissipation ^a	P_D	2	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{Sg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70718.

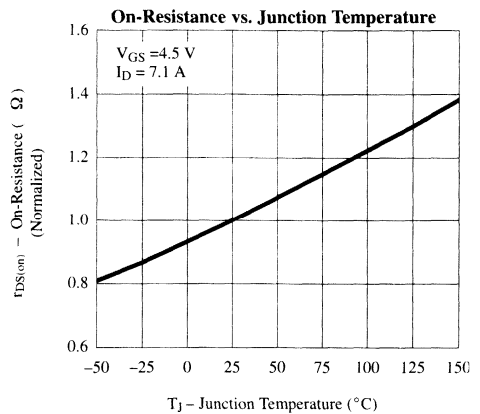
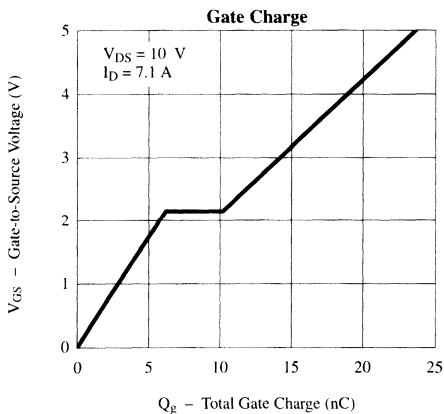
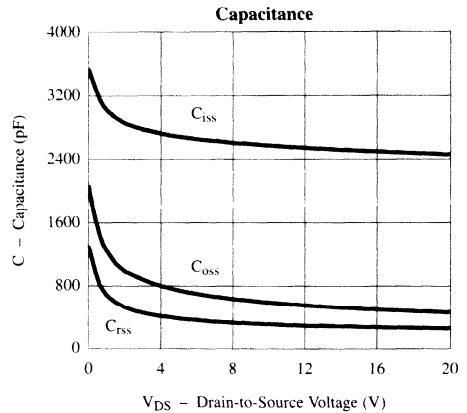
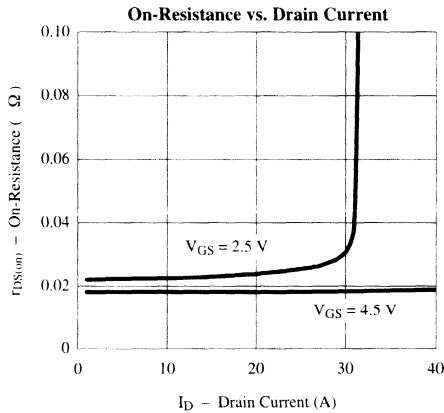
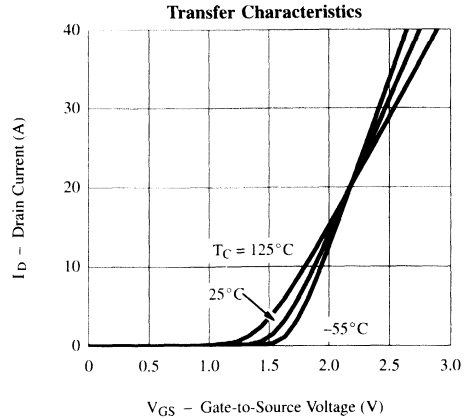
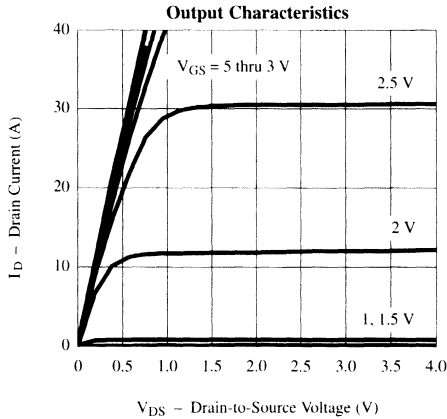
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 7.1\ \text{A}$		0.019	0.025	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 6.0\ \text{A}$		0.025	0.035	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 7.1\ \text{A}$		27		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 7.1\ \text{A}$		25	50	nC
Gate-Source Charge	Q_{gs}			6.5		
Gate-Drain Charge	Q_{gd}			4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		40	60	ns
Rise Time	t_r			40	60	
Turn-Off Delay Time	$t_{d(off)}$			90	150	
Fall Time	t_f			40	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		40	80	

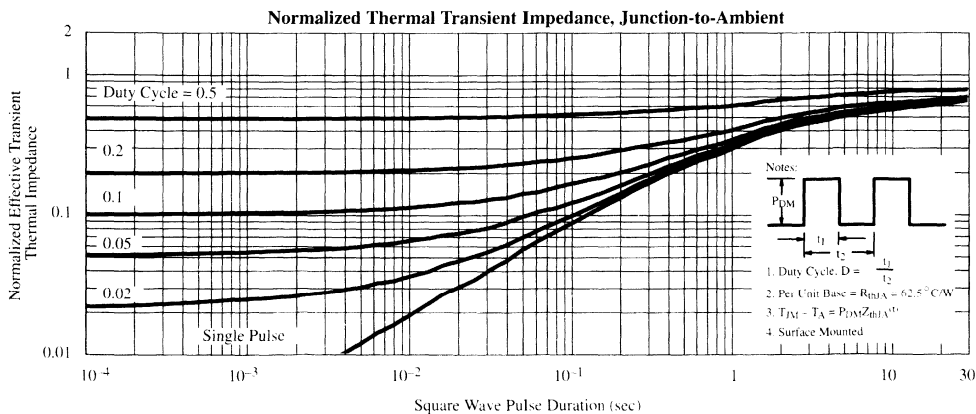
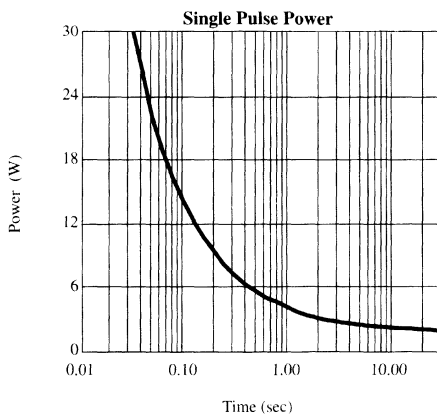
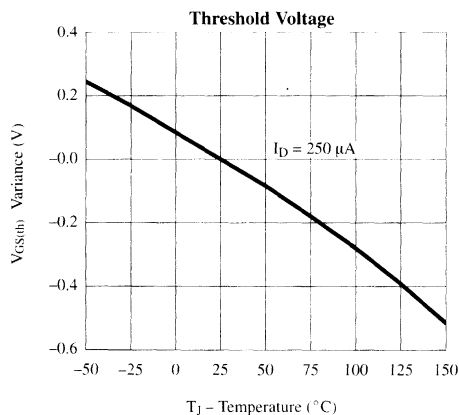
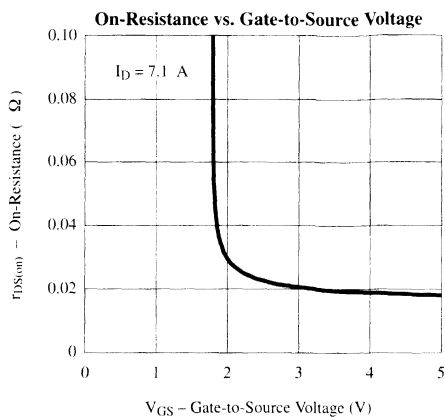
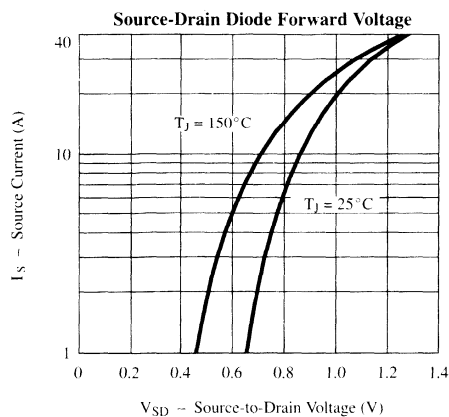
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

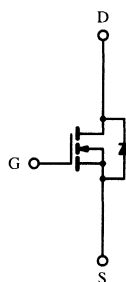
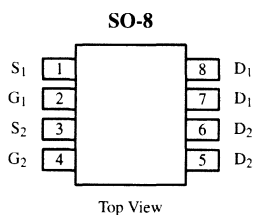


Dual N-Channel 80-V Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
80	0.075 @ V _{GS} = 10 V	± 3.7
	0.095 @ V _{GS} = 6.0 V	± 3.2

TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	80	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 3.7	A
		± 2.9	
Pulsed Drain Current	I _{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I _S	1.7	
Maximum Power Dissipation ^a	P _D	2.0	W
		1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70646.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

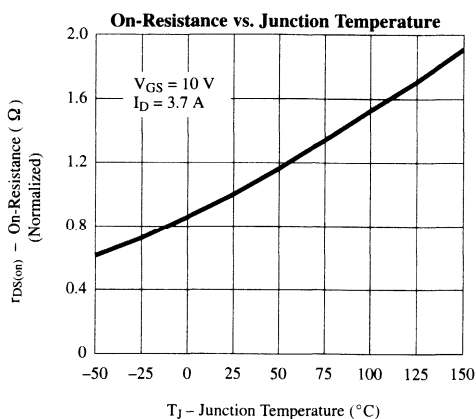
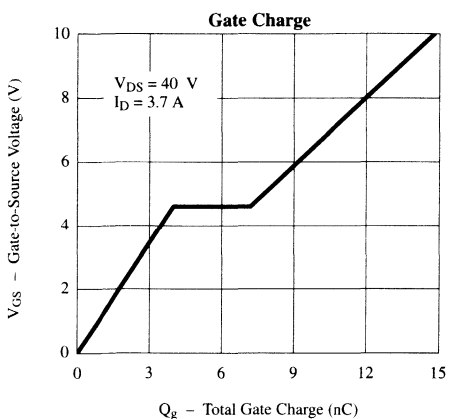
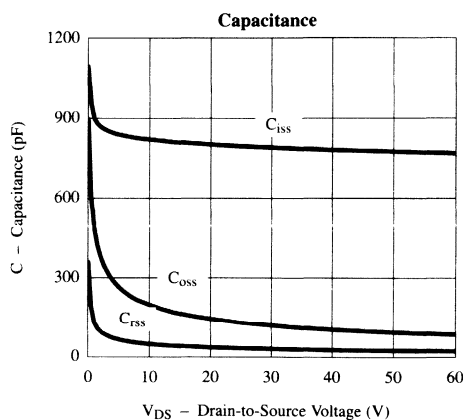
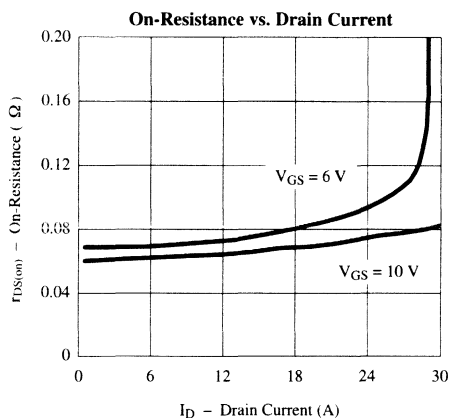
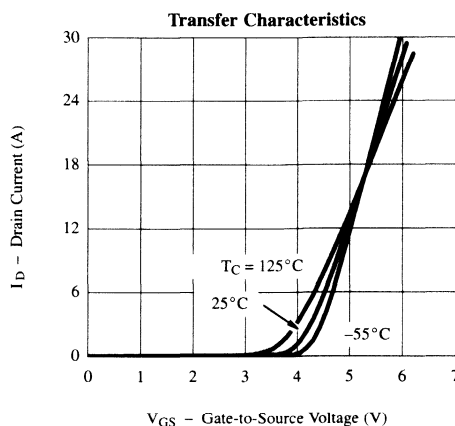
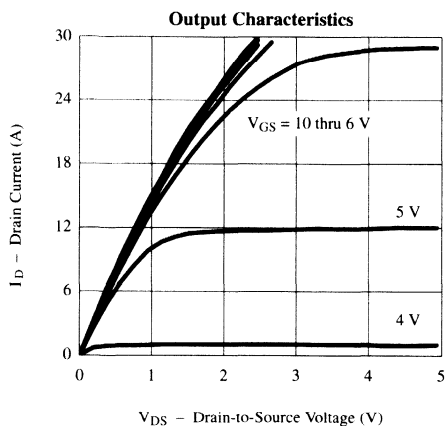
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 3.7\ \text{A}$		0.062	0.075	Ω
		$V_{GS} = 6.0\ \text{V}, I_D = 3.2\ \text{A}$		0.071	0.095	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 3.7\ \text{A}$		12		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 40\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 3.7\ \text{A}$		15	30	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			3.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\ \text{V}, R_L = 40\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		75	110	

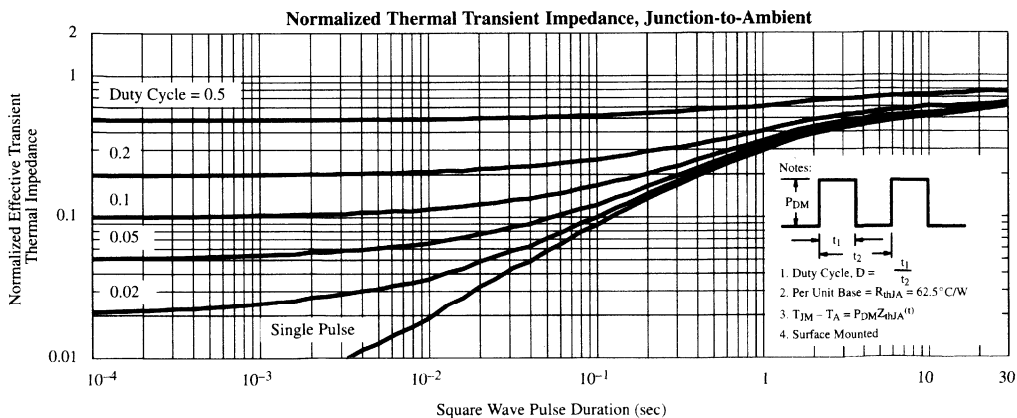
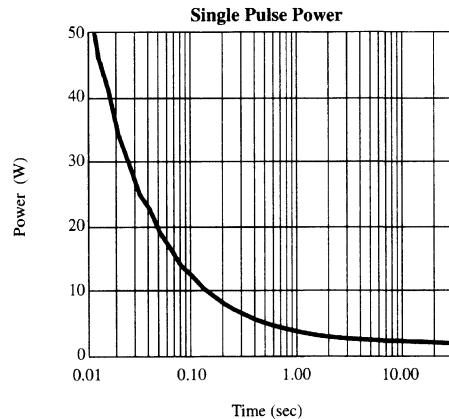
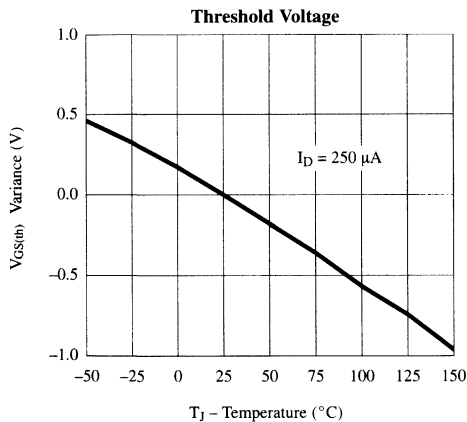
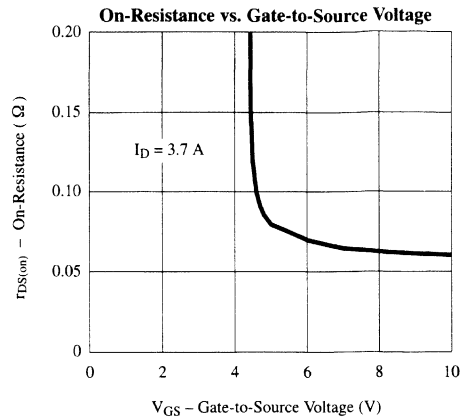
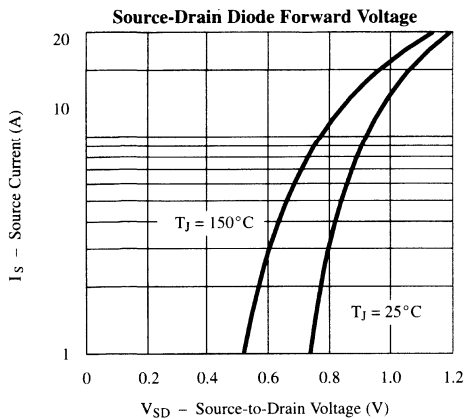
Notes

a. For design aid only; not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



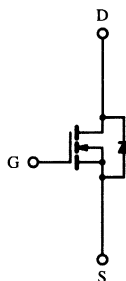
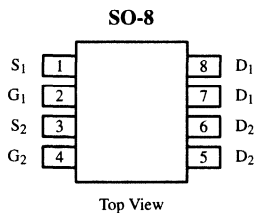
Typical Characteristics (25°C Unless Otherwise Noted)


Dual N-Channel 100-V (D-S) Rated MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
100	0.150 @ V _{GS} = 10 V	± 2.6
	0.180 @ V _{GS} = 6 V	± 2.4

TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C) ^a	I _D	± 2.6	A
		± 2.1	
Pulsed Drain Current	I _{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I _S	1.7	W
Maximum Power Dissipation ^a	P _D	2.0	
		1.3	
Operating Junction and Storage Temperature Range	T _J , T _{sig}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70748.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

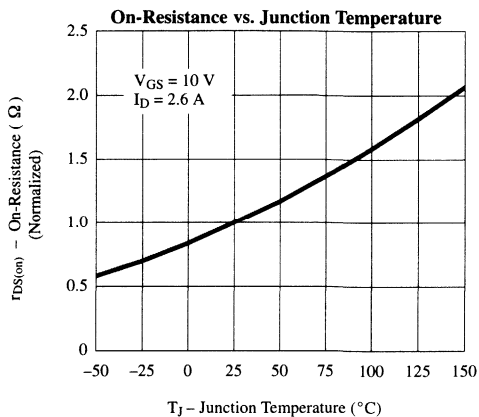
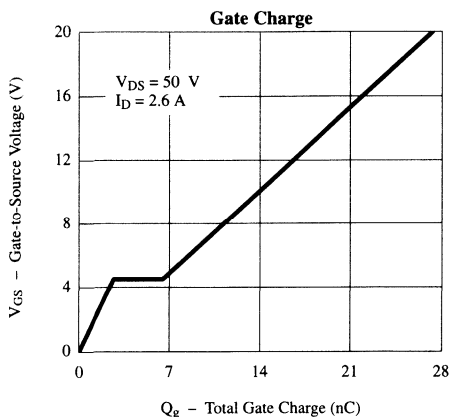
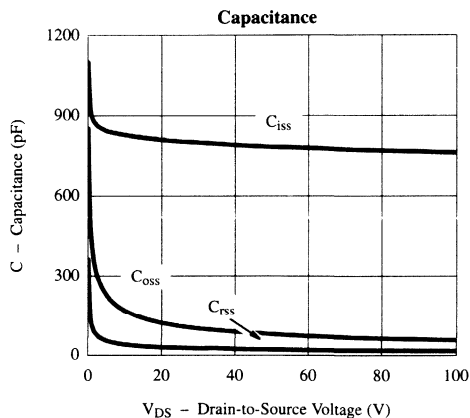
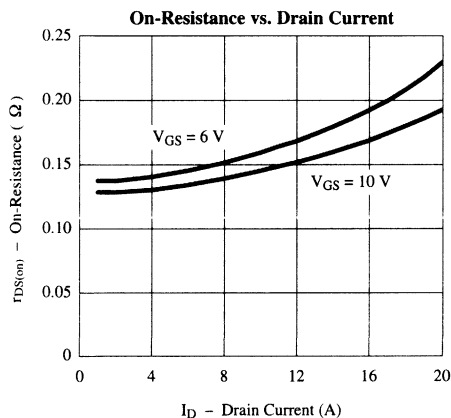
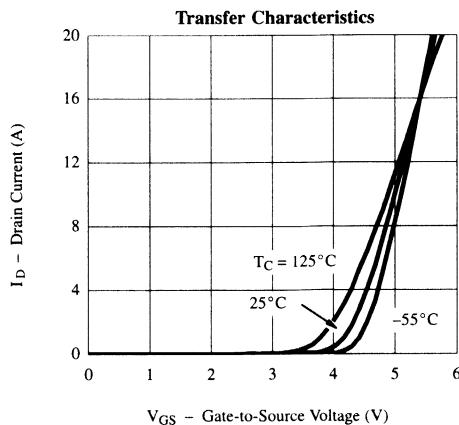
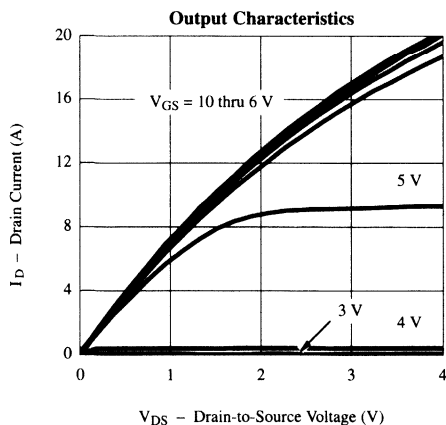
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 100\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	15			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 2.6\ \text{A}$		0.130	0.150	Ω
		$V_{GS} = 6\ \text{V}, I_D = 2.4\ \text{A}$		0.140	0.180	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 2.6\ \text{A}$		11		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 2.6\ \text{A}$		15	30	nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			4.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ \text{V}, R_L = 50\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	90	

Notes

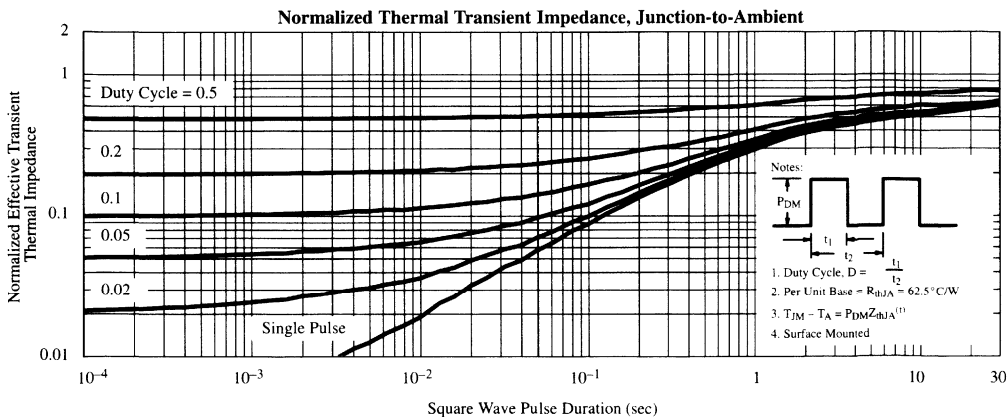
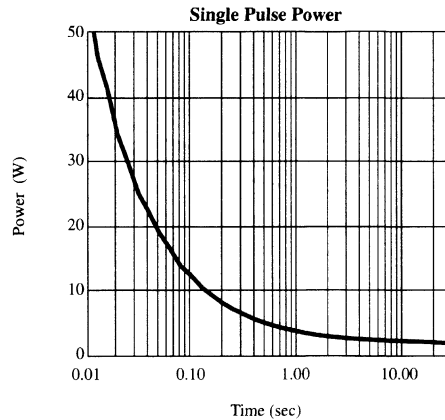
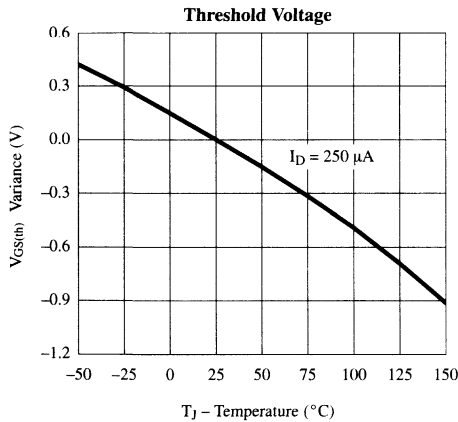
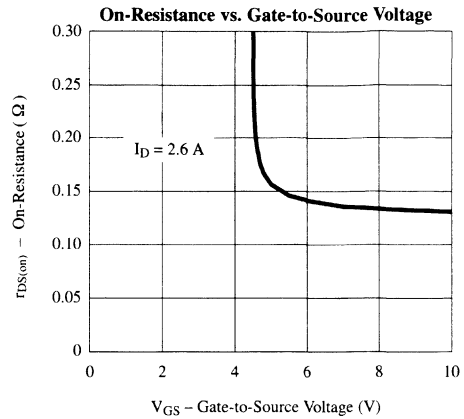
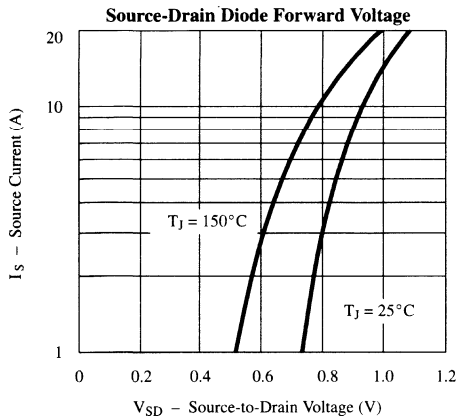
a. For design aid only; not subject to production testing.

 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



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SOIC-8

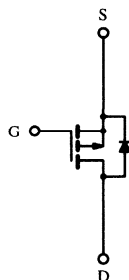
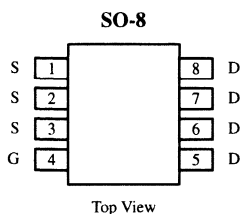
Typical Characteristics (25°C Unless Otherwise Noted)


P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.025 @ $V_{GS} = -4.5$ V	± 7.7
	0.033 @ $V_{GS} = -2.5$ V	± 6.6

2.5-V Rated



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 7.7	A
	$T_A = 70^\circ\text{C}$		± 6.2	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a		I_S	-2.3	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70164.

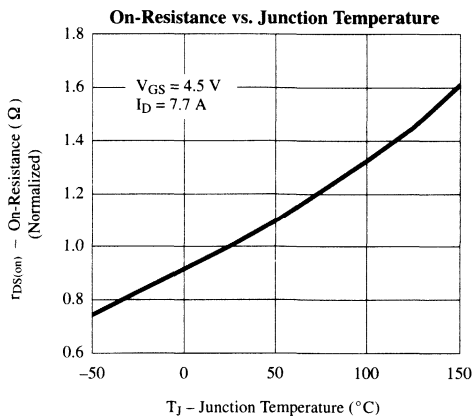
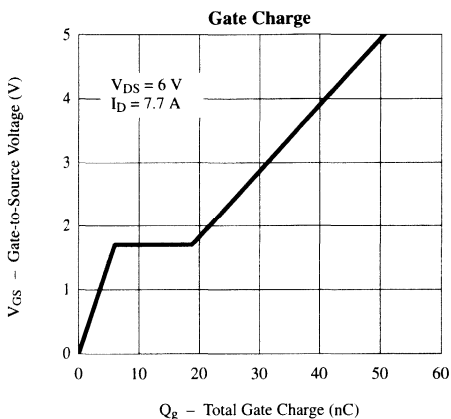
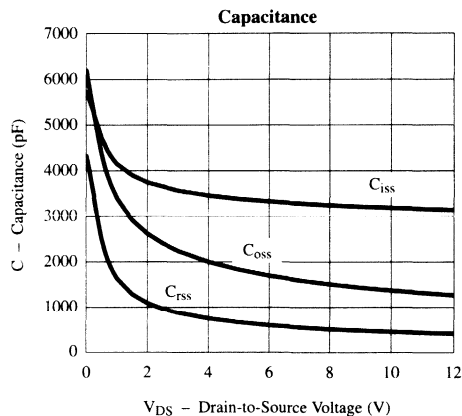
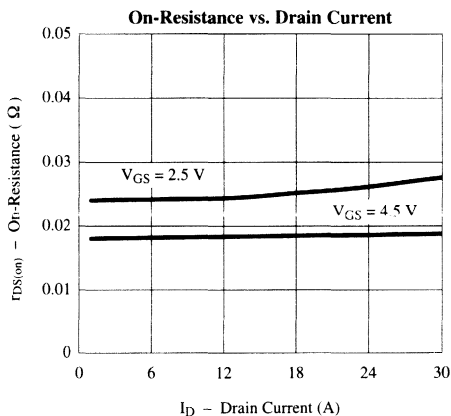
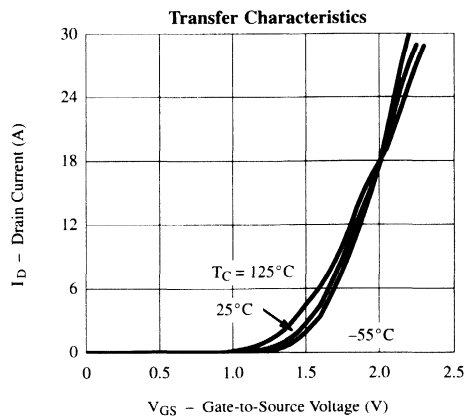
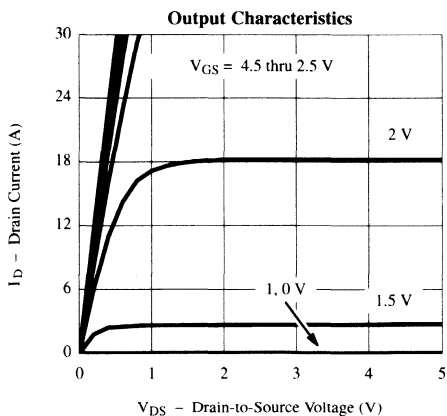
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -12\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-30			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -7.7\ \text{A}$		0.019	0.025	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -6.6\ \text{A}$		0.024	0.033	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -7.7\ \text{A}$		25		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.3\ \text{A}, V_{GS} = 0\ \text{V}$		-0.72	-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -6\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -7.7\ \text{A}$		46	80	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			13		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\ \text{V}, R_L = 6\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		40	80	ns
Rise Time	t_r			65	130	
Turn-Off Delay Time	$t_{d(off)}$			240	400	
Fall Time	t_f			140	250	
Source-Drain Reverse Recovery Time	t_{rr}			70	120	

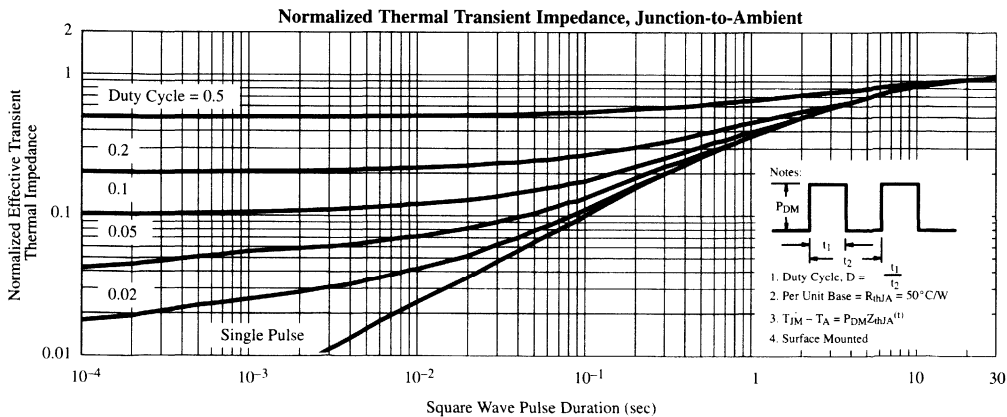
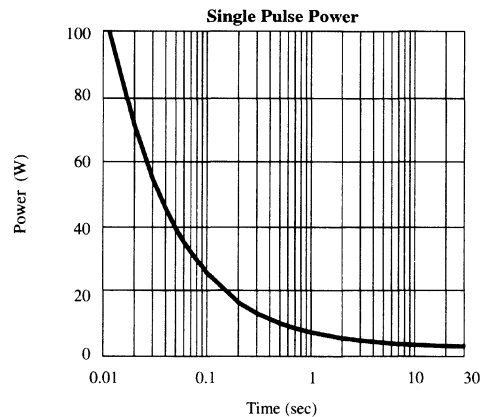
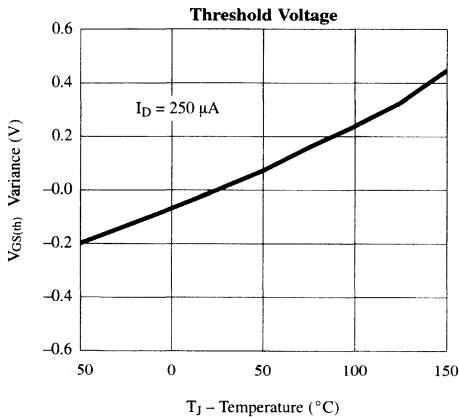
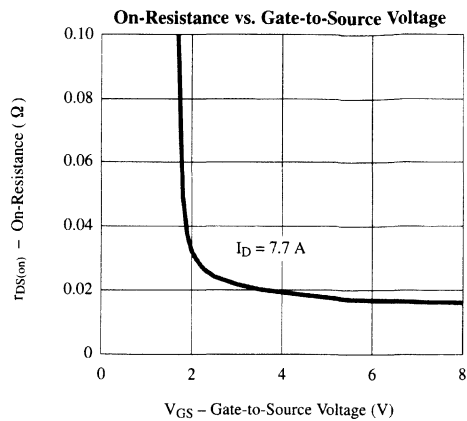
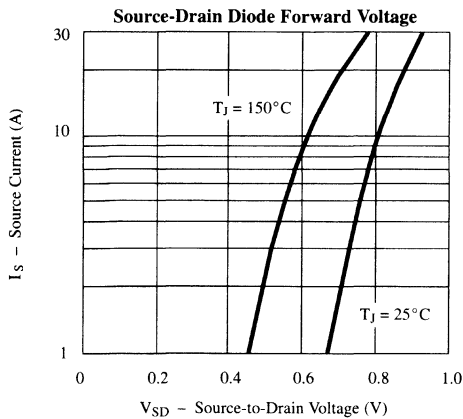
Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)



Application Specific Standard MOSFETs (ASSM)

4

Selector Guides

TSOP-6

TSSOP-8

SOIC-8

Appendix

Worldwide Sales Offices and Distributors

Dual-Gate Power MOSFETs Improve Light-Load Efficiency in DC/DC Converters

To minimize losses, PWM designers and MOSFET manufacturers have historically focused on lowering on-resistance. But higher switching frequencies and the efficiency demands of battery-powered circuits no longer allow gate charge and switching speed issues to be ignored. Particularly at light-load currents where resistive losses are minimal, the most significant component of loss is often associated with the gate drive of the MOSFET.

Light-load efficiency concerns have in the past been handled by variable frequency designs or some type of pulse-frequency modulation (PFM) scheme. But any variable frequency mode creates a variable frequency noise spectrum, which can be of great concern to designers of cell phones and other communications systems.

A solution to this problem is the dual-efficiency MOSFET from TEMIC Semiconductors. This power MOSFET allows high efficiencies across large or bi-modal load ranges while enabling the designer to use a constant frequency control scheme. Cellular phones are a good example of a bi-modal load range, where transmission involves several amps of current and standby mode involves several milliamps of current.

TEMIC's dual-efficiency MOSFET is effectively two MOSFETs of dissimilar area on the same die connected with parallel sources and drains but separate gates. In dc-to-dc conversion circuits, these two MOSFETs operate in tandem during high-load conditions, but are switched so that only the smaller MOSFET operates during light-load conditions. This reduces the gate losses while increasing efficiency during light loads. It should be noted that as the smaller MOSFET is on the same die as the larger MOSFET, its thermal dissipation area is dramatically increased compared to a single-MOSFET device of the same size. Hence, the dual-efficiency MOSFET gives much higher efficiencies in a light-load mode than two discrete MOSFETs of similar on-resistance connected in parallel.

TEMIC's dual-efficiency MOSFETs can be used in any topology. Figure 1 shows a block diagram of a boost converter with efficiency results.

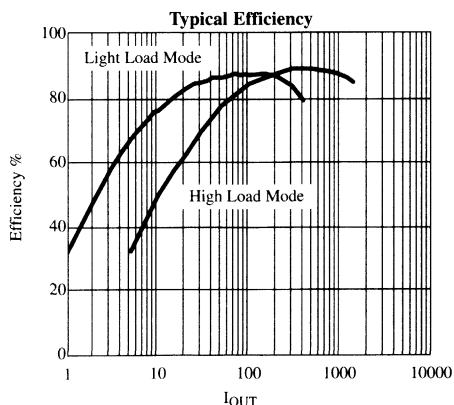
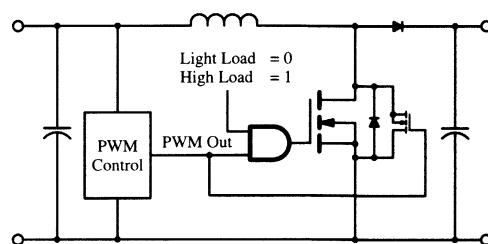


Figure 1. Boost Converter Using Dual Efficiency MOSFET with Typical Efficiency Plot

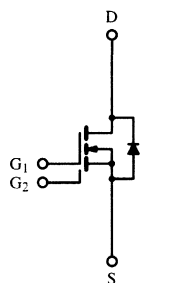
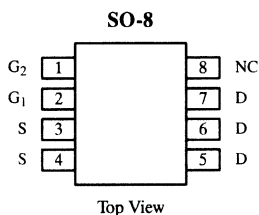


N-Channel 30:1 Ratio Dual-Gate 30-V (D-S) MOSFET

Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
Gate 1	30	0.022 @ V _{GS} = 10 V	± 7.7
		0.03 @ V _{GS} = 4.5 V	± 6.4
Gate 2		0.25 @ V _{GS} = 10 V	± 2.0
		0.40 @ V _{GS} = 4.5 V	± 1.5

TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Gate 1	Gate 2	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 7.7	± 6.4	A
	T _A = 70°C		± 4.4	± 6.0	
Pulsed Drain Current		I _{DM}	± 40	± 4.0	
Continuous Source Current (Diode Conduction) ^a		I _S	2		W
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.3		
	T _A = 70°C		1.0		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	55	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

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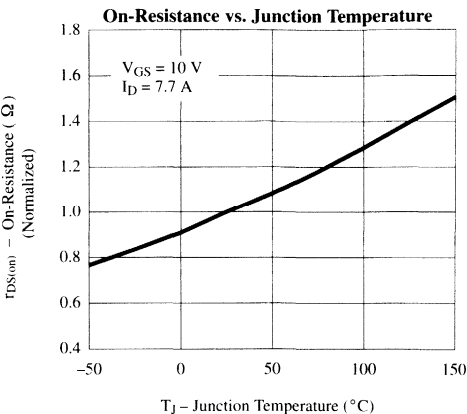
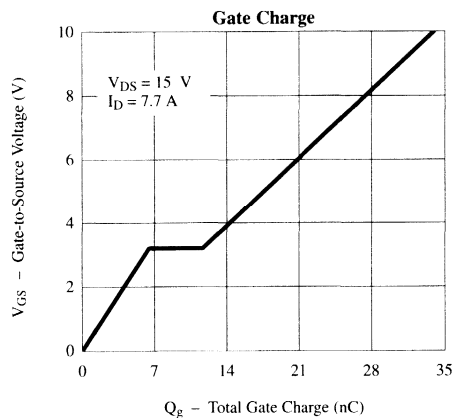
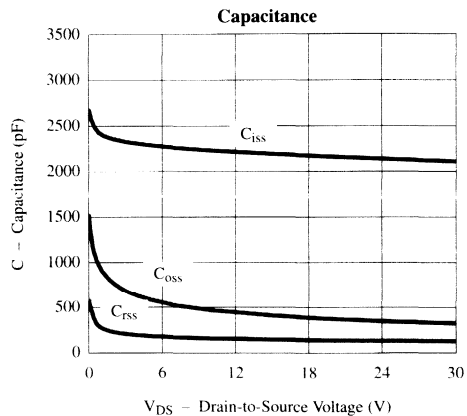
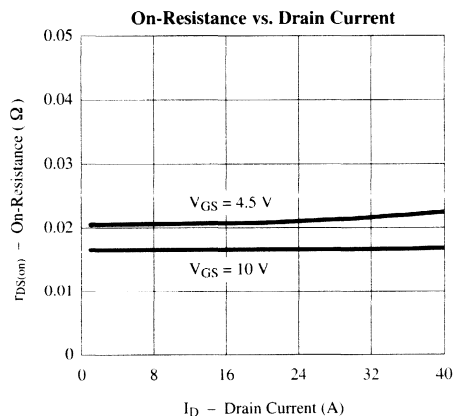
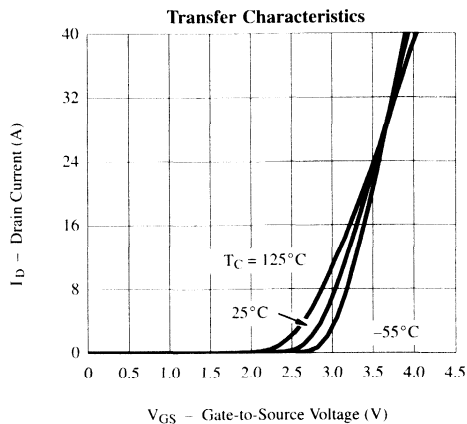
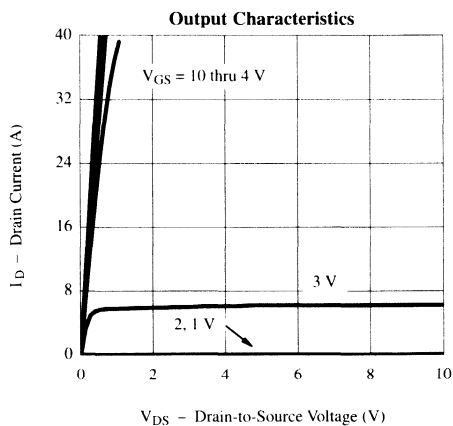
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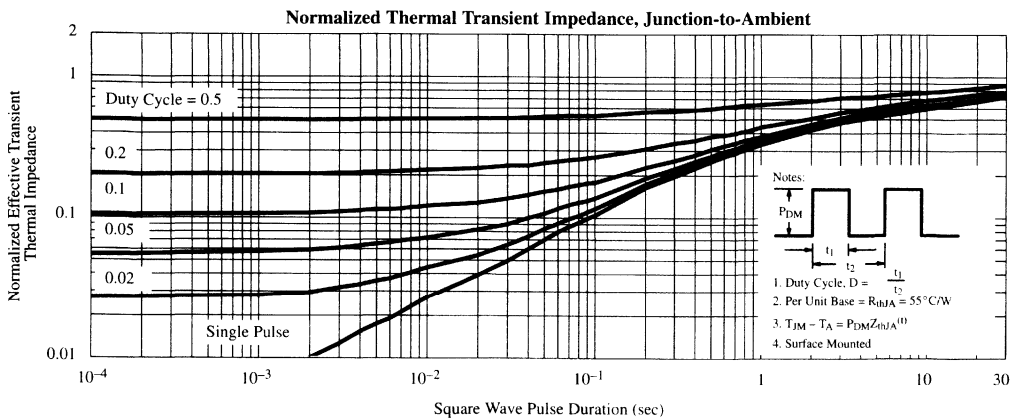
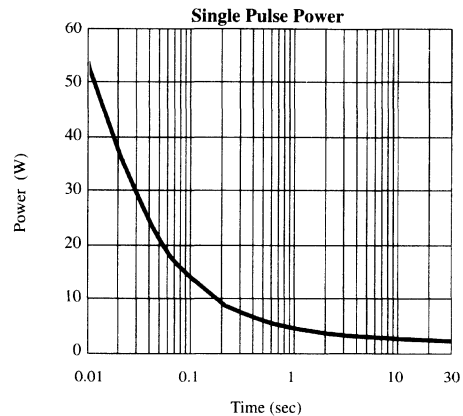
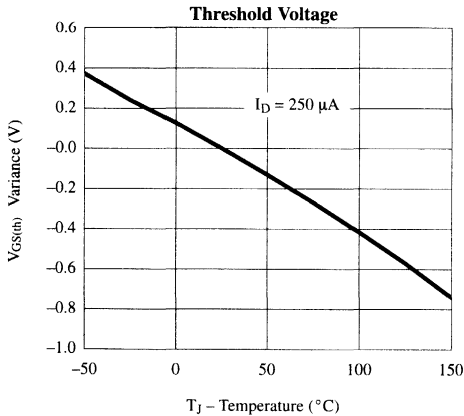
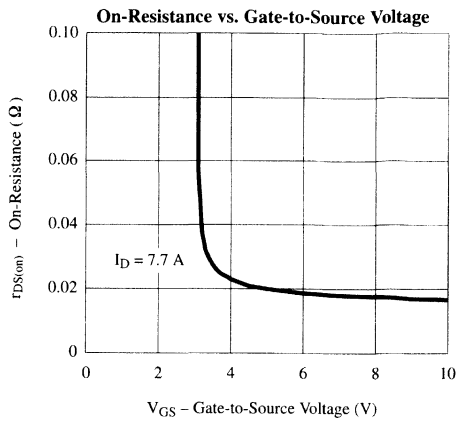
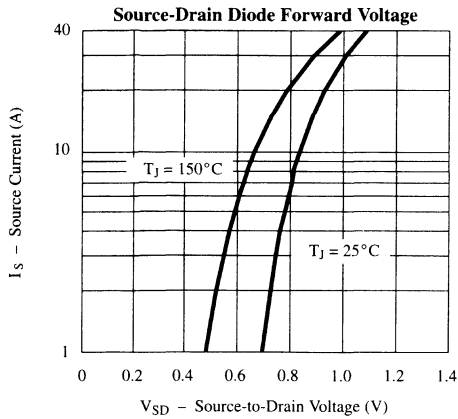
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1			V	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55°C			5		
On-State Drain Current ^a	I _{D(on)}	(G ₁ = G ₂) V _{DS} = 5 V, V _{GS} = 10 V	40			A	
Drain-Source On-State Resistance ^a	r _{DS1(on)}	(G ₁ = G ₂) V _{GS} = 10 V, I _D = 7.7 A		0.017	0.022	Ω	
		(G ₁ = G ₂) V _{GS} = 4.5 V, I _D = 6.4 A		0.021	0.03		
	r _{DS2(on)}	V _{GS1} = 0 V, V _{GS2} = 10 V, I _D = 2.0 A		0.20	0.25		
		V _{GS1} = 0 V, V _{GS2} = 4.5 V, I _D = 0.3 A		0.30	0.40		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.7 A		21		S	
Diode Forward Voltage ^a	V _{SD}	I _S = 2 A, V _{GS} = 0 V		0.72	1.1	V	
Dynamic ^b							
Total Gate Charge	Q _g	Gate 1 V _{DS} = 15 V, V _{GS(1)} = 10 V, I _D = 7.7 A Gate 2 V _{DS} = 15 V, V _{GS(1)} = 0 V, V _{GS(2)} = 10 V, I _D = 2.0 A	Gate 1		34	60	nC
Gate-Source Charge	Q _{gs}		Gate 2		2.2	5	
			Gate 1		6.5		
Gate-Drain Charge	Q _{gd}		Gate 2		0.5		
		Gate 1		5.2			
		Gate 2		0.28			
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		12	15	ns	
Rise Time	t _r			9	20		
Turn-Off Delay Time	t _{d(off)}			55	80		
Fall Time	t _f			15	30		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs		40	60		

Notes

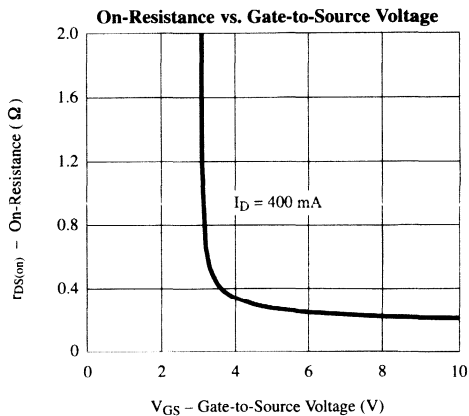
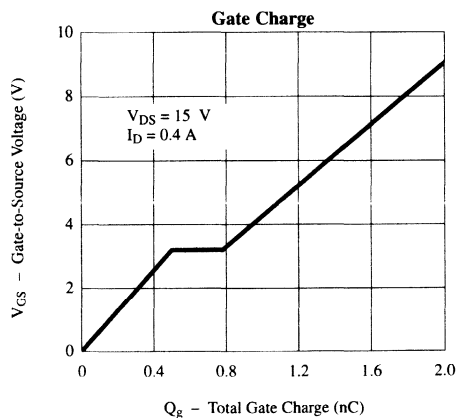
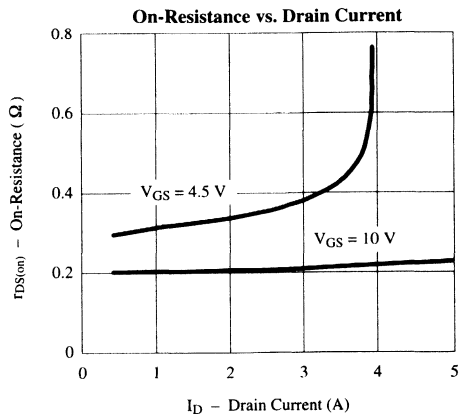
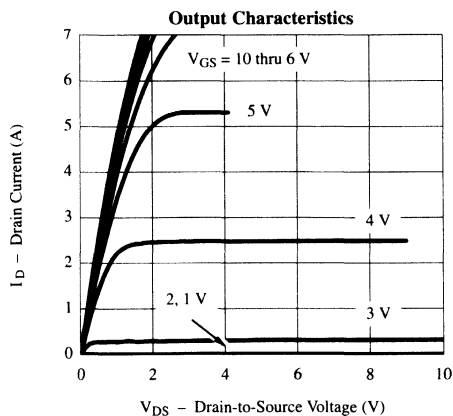
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics ($V_{G1} = V_{G2}$, 25°C Unless Noted)



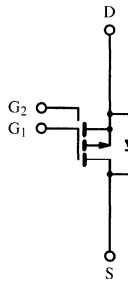
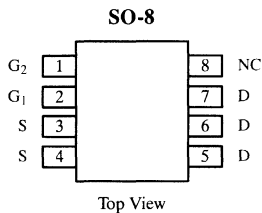
Typical Characteristics ($V_{G1} = V_{G2}$, 25°C Unless Otherwise Noted)


Typical Characteristics ($V_{G1} = 0$ V, 25°C Unless Noted)



P-Channel 30:1 Ratio Dual-Gate 30-V (D-S) MOSFET
Product Summary

	V_{DS} (V)	r_{DS(on)} (Ω)	I_D (A)
Gate 1	-30	0.035 @ V _{GS} = -10 V	± 6
		0.054 @ V _{GS} = -4.5 V	± 4.8
Gate 2		1.3 @ V _{GS} = -10 V	± 0.9
		2.2 @ V _{GS} = -4.5 V	± 0.7

TrenchFET™
 Power MOSFETs


P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Gate 1	Gate 2	Unit
Drain-Source Voltage		V _{DS}	-30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 6	± 0.9	A
	T _A = 70°C		± 4.8	± 0.7	
Pulsed Drain Current		I _{DM}	± 30	± 1.5	
Continuous Source Current (Diode Conduction) ^a		I _S	-1.25		
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.3		W
	T _A = 70°C		1.0		
Operating Junction and Storage Temperature Range		T _J , T _{sig}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	55	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

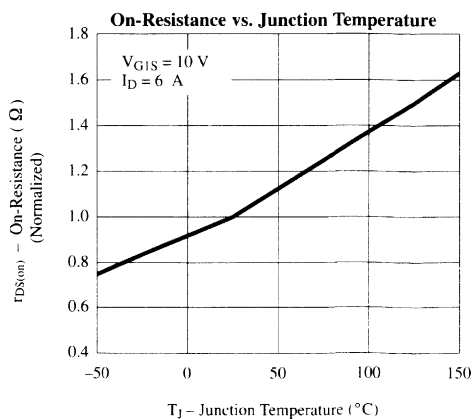
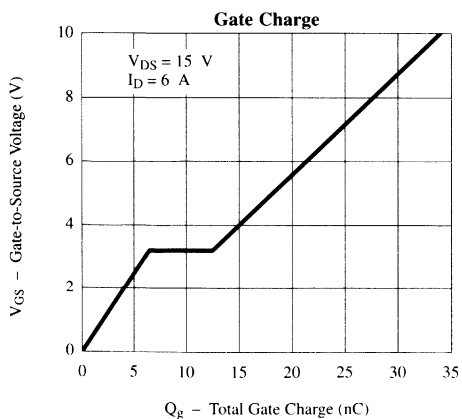
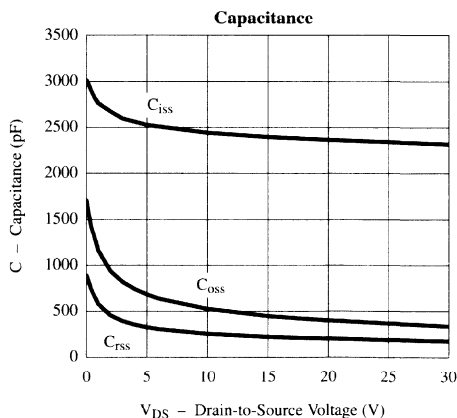
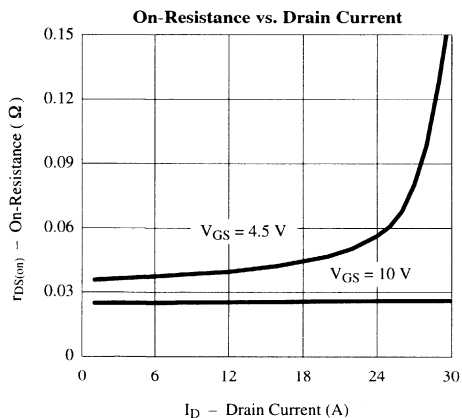
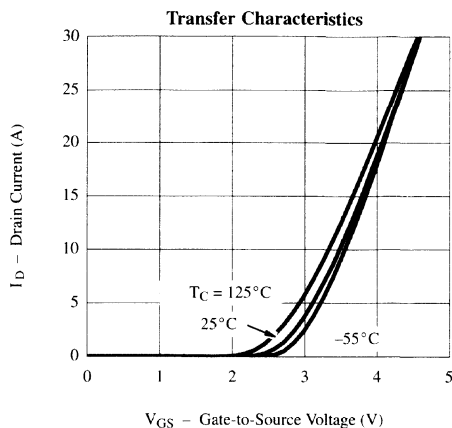
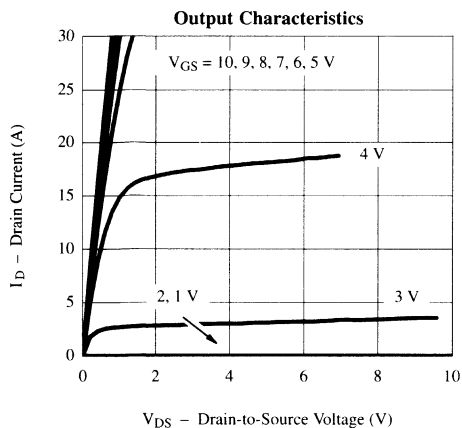
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Specifications (T_J = 25°C Unless Otherwise Noted)

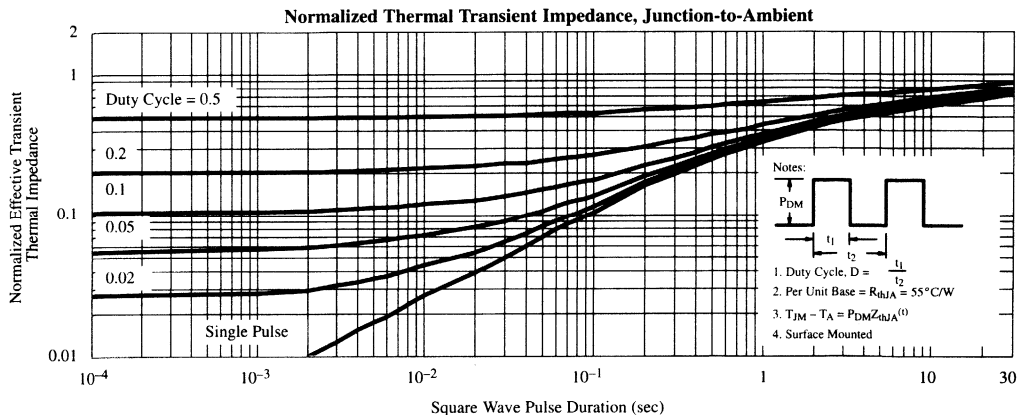
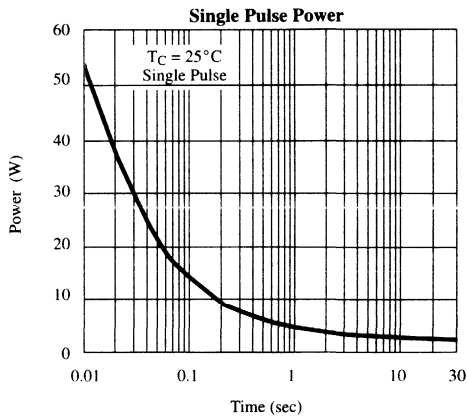
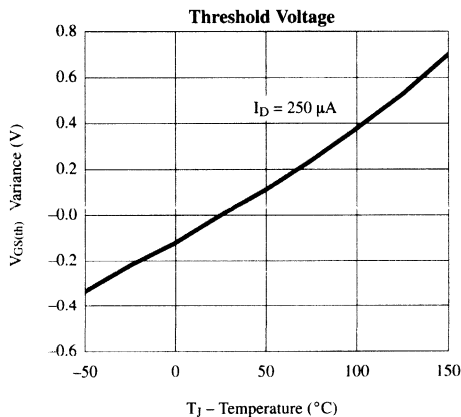
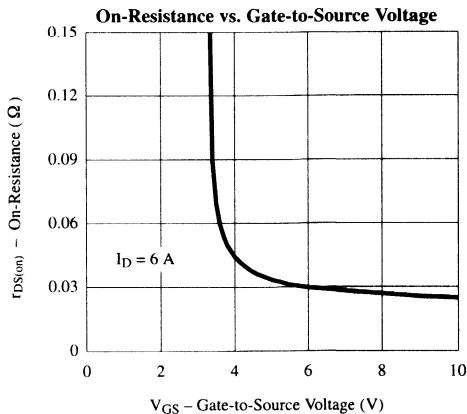
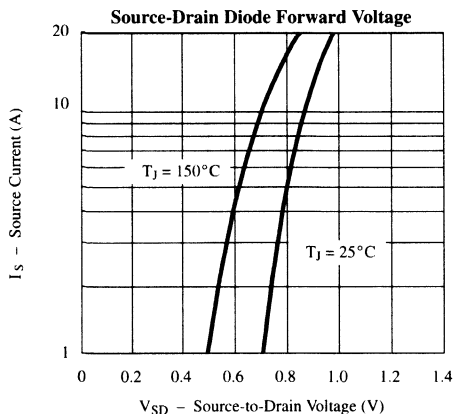
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit		
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1			V		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA		
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55°C			-5			
On-State Drain Current ^a	I _{D(on)}	(G ₁ = G ₂) V _{DS} = -5 V, V _{GS} = -10 V	-20			A		
Drain-Source On-State Resistance ^a	r _{DS1(on)}	(G ₁ = G ₂) V _{GS} = -10 V, I _D = -6 A		0.028	0.035	Ω		
		(G ₁ = G ₂) V _{GS} = -4.5 V, I _D = -4.8 A		0.041	0.054			
	r _{DS2(on)}	V _{G1S} = 0 V, V _{G2S} = -10 V, I _D = -0.15 A		1.05	1.3			
		V _{G1S} = 0 V, V _{G2S} = -4.5 V, I _D = -0.1 A		1.65	2.2			
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -6 A		13		S		
Diode Forward Voltage ^a	V _{SD}	I _S = -1.25 A, V _{GS} = 0 V		0.7	-1.1	V		
Dynamic ^b								
Total Gate Charge	Q _g	Gate 1 V _{DS} = -15 V, V _{GS(1, 2)} = -10 V I _D = -6 A Gate 2 V _{DS} = -15 V, V _{GS(1)} = -0 V V _{GS(2)} = -10 V, I _D = -0.15 A	Gate 1		34	60	nC	
Gate-Source Charge	Q _{gs}		Gate 2		2.0	5		
			Gate 1		6.5			
Gate-Drain Charge	Q _{gd}		Gate 2		0.5			
			Gate 1		6.0			
			Gate 2		0.2			
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		15	25	ns		
Rise Time	t _r			11	20			
Turn-Off Delay Time	t _{d(off)}			52	80			
Fall Time	t _f			20	35			
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.25 A, di/dt = -100 A/μs		30	60			

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics ($V_{G1} = V_{G2}$, 25°C Unless Noted)


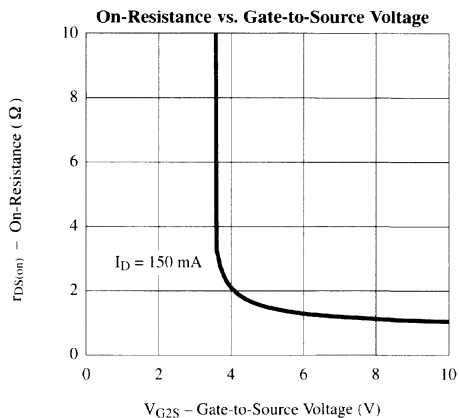
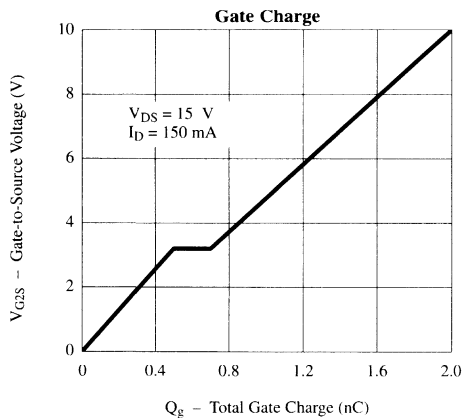
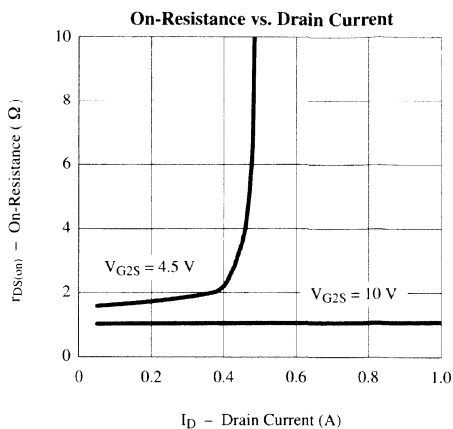
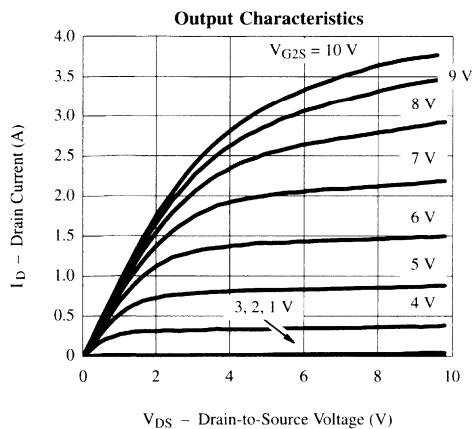
Typical Characteristics ($V_{G1} = V_{G2}$, 25°C Unless Otherwise Noted)



4

Application Specific Standard MOSFETs (ASSM)

Typical Characteristics ($V_{G1} = 0$ V, 25°C Unless Noted)



Power MOSFETs Optimized for Low-Voltage DC/DC Conversion

Designers of low-voltage dc-to-dc converters have two main concerns: reducing size and reducing losses. As a way of reducing size, designers are increasing switching frequencies. But the result has often been reduced converter efficiency. To minimize losses, MOSFET manufacturers have generally focused on lowering on-resistance. But the results have not been optimal for dc-to-dc conversion designs, since gate charge and switching speed issues have been largely ignored. The dominant losses associated with MOSFETs were once conduction losses, but this is no longer the case.

TEMIC's new family of PWM optimized MOSFETs are designed to give the highest efficiency available for a given on-resistance in switching applications such as dc-to-dc conversion. These new devices provide a very low gate charge per unit of on-resistance, in addition to fast switching times. The result is reduced gate drive and crossover losses, allowing designers of dc-to-dc converters to simultaneously to reduce design size and increase efficiency.

Figure of Merit for PWM Optimized MOSFET Technology

Normalized gate charge serves as a quick figure of merit for comparing the PWM optimized, conventional, and low-threshold MOSFET technologies. This was calculated by normalizing the on-resistance and gate charge of the n-channel MOSFET to 100 m Ω :

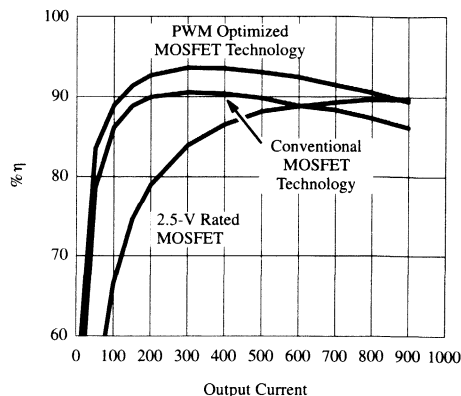
Type of MOSFET	Typical On-Resistance at 4.5 V (m Ω)	Specific Gate Charge	Normalized Gate Charge per 100 m Ω (nC)
PWM Optimized	120	1.7	1.4
Conventional	100	4.0	4.0
2.5-V Rated	73	16.0	22.0

Similar performance advantages will be seen for the p-channel process as well.

Ideal applications for TEMIC's PWM optimized MOSFETs include mobile communication equipment and other hand-held battery-operated systems. An example of the efficiency gains achieved with this technology is shown below.

Efficiency comparison between high-frequency, conventional, and low-threshold MOSFETs at a switching frequency of 1 MHz.

If you would like to review a detailed application note, call our FaxBack system at 408-970-5600 and refer to document number 70649.

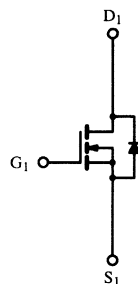
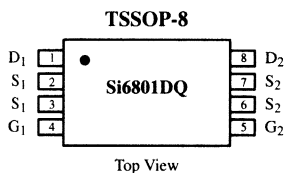


Dual N- and P-Channel, Reduced Q_g , Fast Switching MOSFET

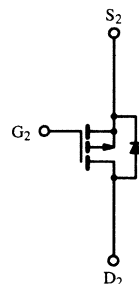
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.160 @ $V_{GS} = 4.5$ V	± 1.9
		0.260 @ $V_{GS} = 3.0$ V	± 1.5
P-Channel	-20	0.190 @ $V_{GS} = -4.5$ V	± 1.7
		0.280 @ $V_{GS} = -3.0$ V	± 1.3

High-Efficiency
PWM Optimized



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	−20	V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 1.9	± 1.7	A
	T _A = 70°C		± 1.5	± 1.3	
Pulsed Drain Current		I _{DM}	± 8		
Continuous Source Current (Diode Conduction) ^a		I _S	1.0	−1.0	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	1.0		W
	T _A = 70°C		0.64		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70187.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

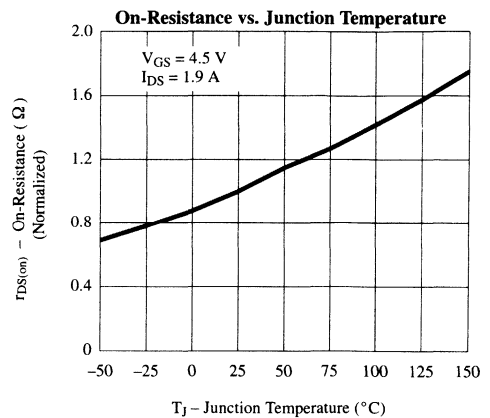
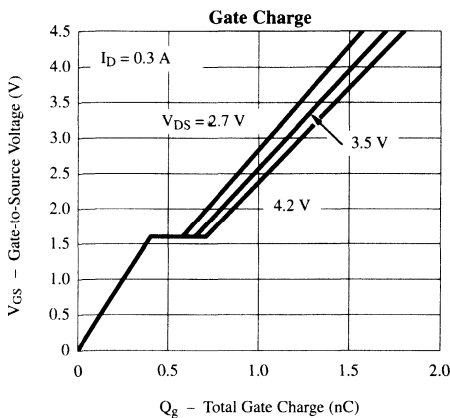
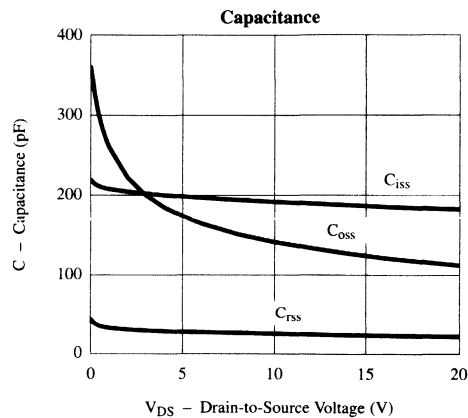
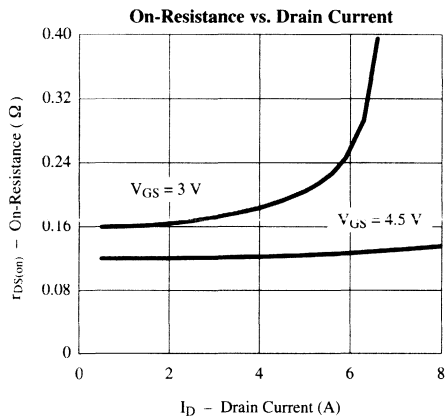
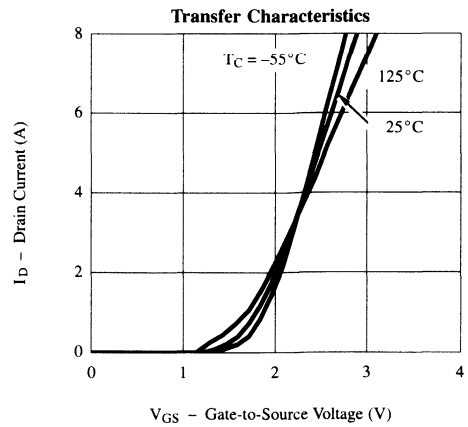
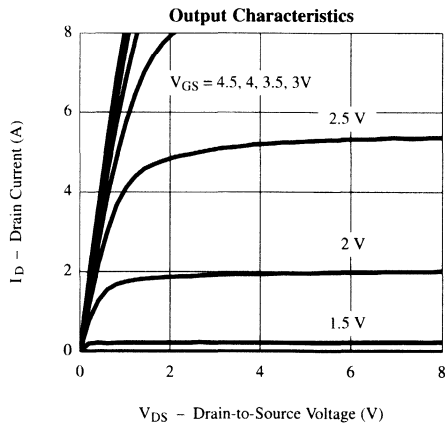
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	N-Ch	0.6		V
		$V_{DS} = V_{GS}, I_D = -250\ \mu A$	P-Ch	-0.6		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V, V_{GS} = \pm 12\ V$	N-Ch P-Ch		± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ V, V_{GS} = 0\ V$	N-Ch		1	μA
		$V_{DS} = -20\ V, V_{GS} = 0\ V$	P-Ch		-1	
		$V_{DS} = 20\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	N-Ch		25	
		$V_{DS} = -20\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	P-Ch		-25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ V, V_{GS} = 4.5\ V$	N-Ch	6		A
		$V_{DS} = -5\ V, V_{GS} = -4.5\ V$	P-Ch	-6		
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ V, I_D = 1.9\ A$	N-Ch		0.120	Ω
		$V_{GS} = -4.5\ V, I_D = 1.7\ A$	P-Ch		0.155	
		$V_{GS} = 3.0\ V, I_D = 1.5\ A$	N-Ch		0.160	
		$V_{GS} = -3.0\ V, I_D = 1.3\ A$	P-Ch		0.210	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ V, I_D = 1.9\ A$	N-Ch		5.4	S
		$V_{DS} = -15\ V, I_D = -1.7\ A$	P-Ch		4.0	
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.0\ A, V_{GS} = 0\ V$	N-Ch		0.77	V
		$I_S = -1.0\ A, V_{GS} = 0\ V$	P-Ch		-0.77	
Dynamic ^a						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 3.5\ V, V_{GS} = 4.5\ V, I_D = 0.3\ A$ P-Channel $V_{DS} = -3.5\ V, V_{GS} = -4.5\ V$ $I_D = -0.3\ A$	N-Ch		1.7	nC
Gate-Source Charge	Q_{gs}		P-Ch		3.5	
			N-Ch		0.26	
Gate-Drain Charge	Q_{gd}		P-Ch		0.76	
		N-Ch		0.41		
Turn-On Delay Time	$t_{d(on)}$	P-Ch		0.70		
		N-Ch		7.3	15	ns
Rise Time	t_r	P-Ch		6.0	15	
		N-Ch		10.0	20.0	
Turn-Off Delay Time	$t_{d(off)}$	P-Ch		10.0	20.0	
		N-Ch		11.0	20.0	
Fall Time	t_f	P-Ch		10.0	20.0	
		N-Ch		6.0	15	
Source-Drain Reverse Recovery Time	t_{rr}	P-Ch		7.0	15	
		N-Ch		31	60	
		P-Ch		35	60	

Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

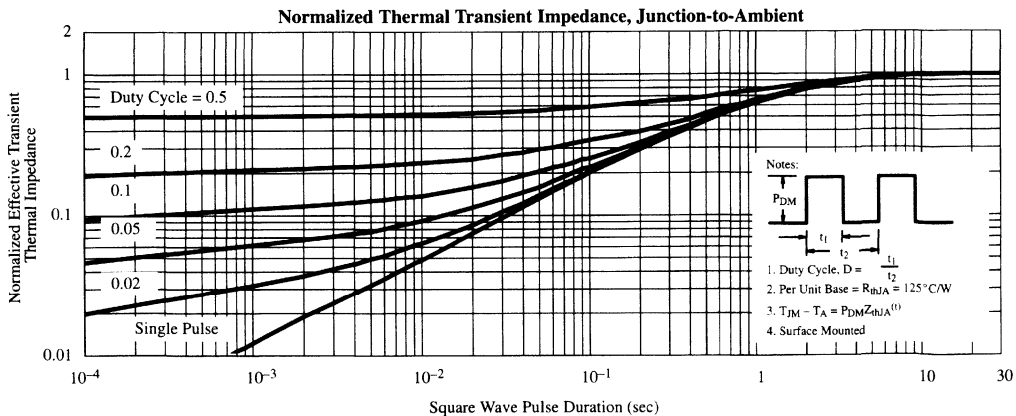
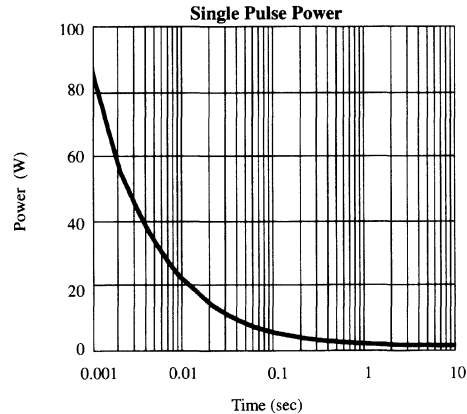
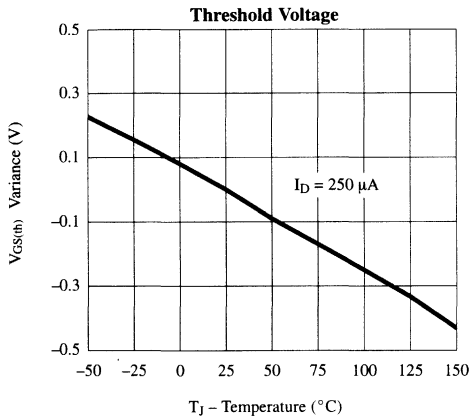
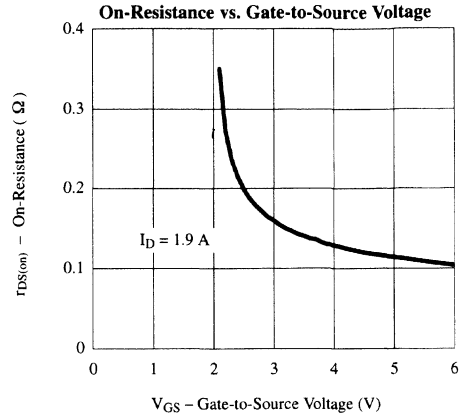
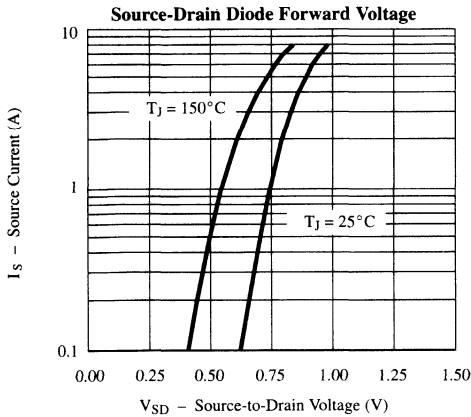
Typical Characteristics (25°C Unless Noted)

N-Channel



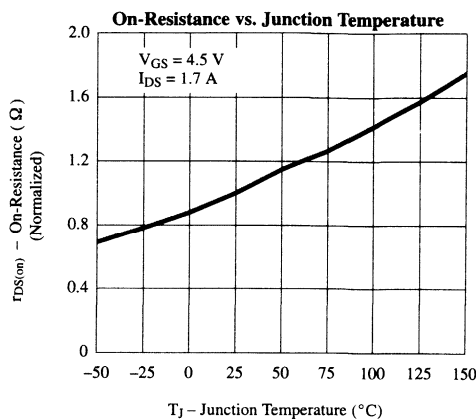
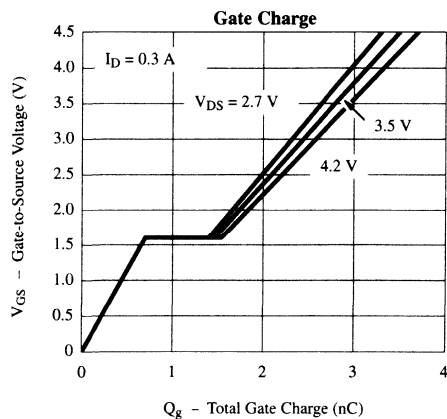
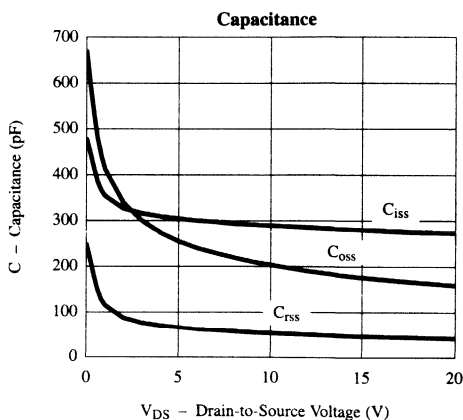
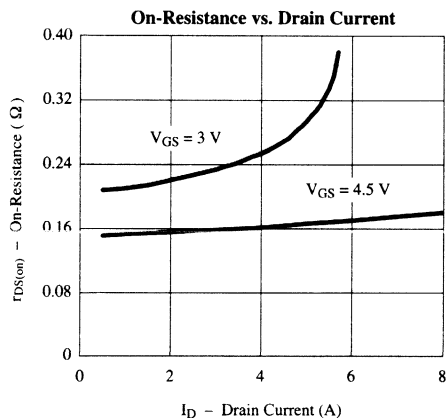
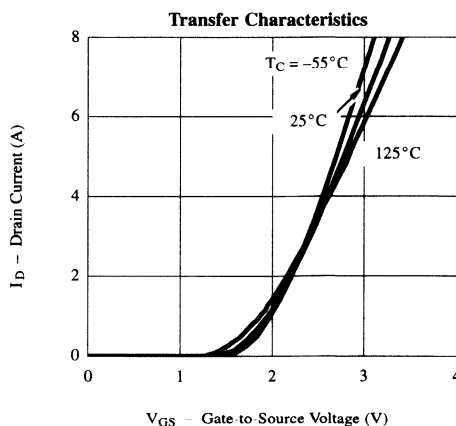
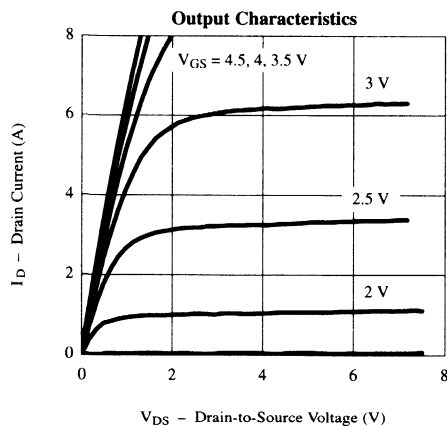
Typical Characteristics (25°C Unless Noted)

N-Channel



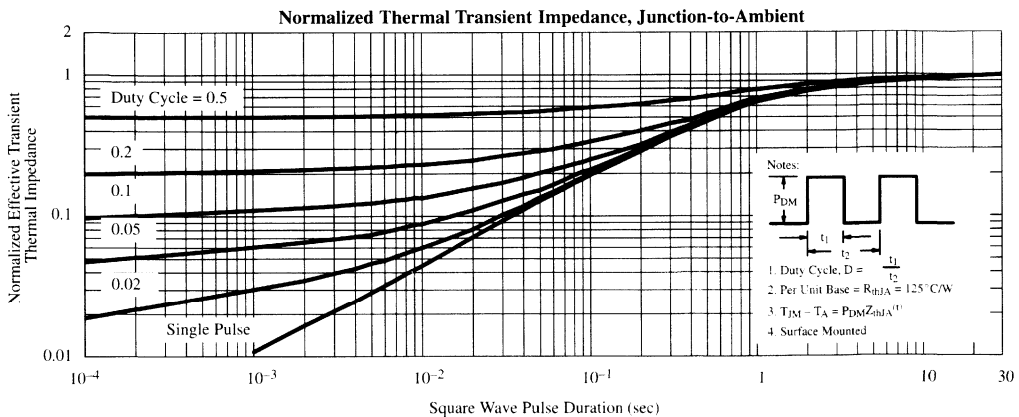
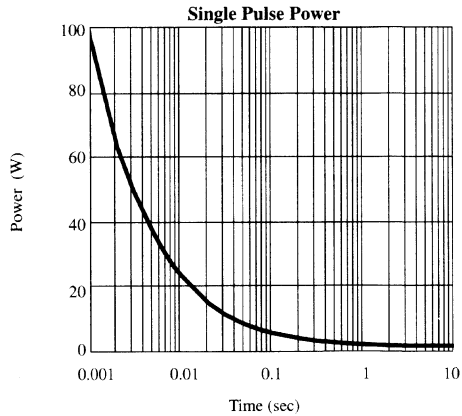
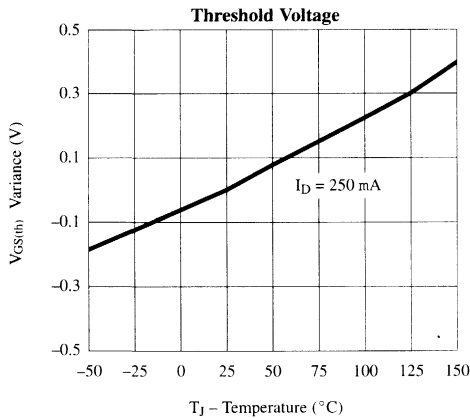
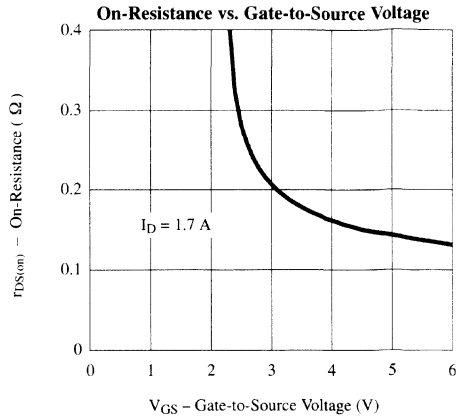
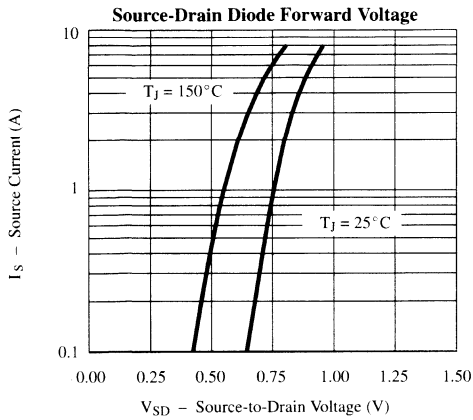
Typical Characteristics (25°C Unless Noted)

P-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

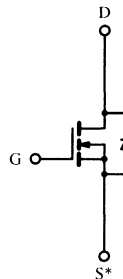
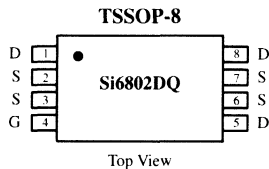


N-Channel, Reduced Q_g , Fast Switching MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.075 @ $V_{GS} = 4.5$ V	± 3.3
	0.110 @ $V_{GS} = 3.0$ V	± 2.7

High-Efficiency
PWM Optimized



*Source Pins 2, 3, 6, and 7 must be tied common.

N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 3.3	A
		± 2.6	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	1.25	
Maximum Power Dissipation ^a	P_D	1.5	W
		1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	83	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

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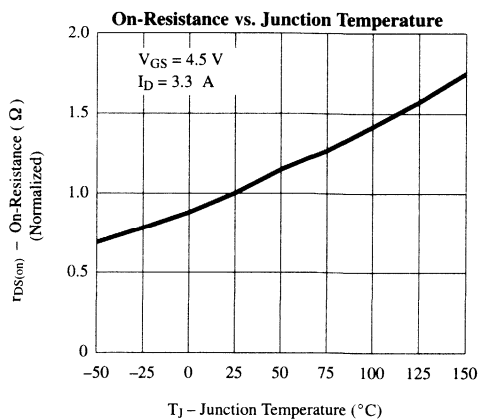
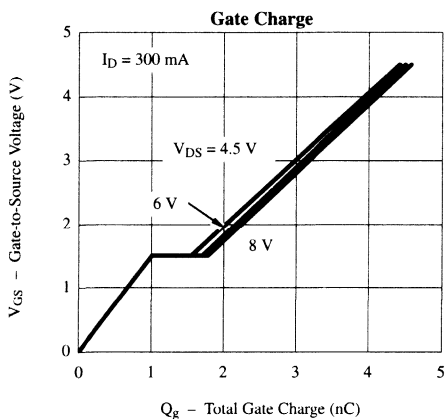
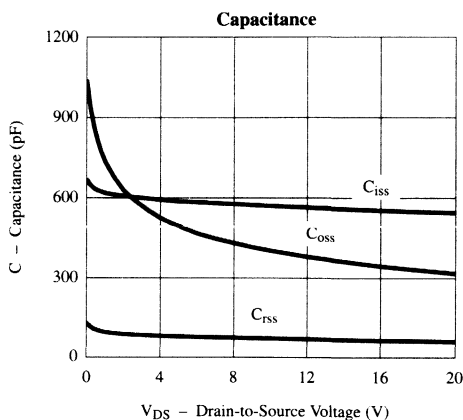
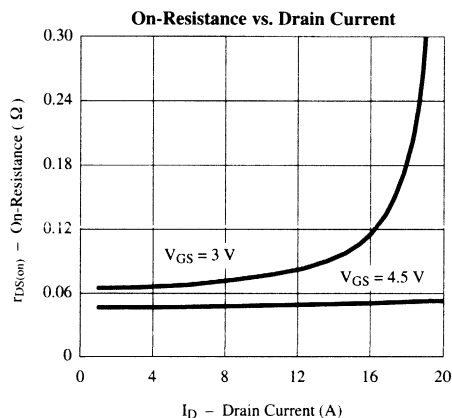
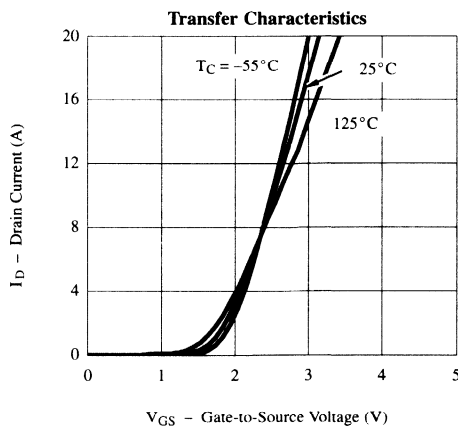
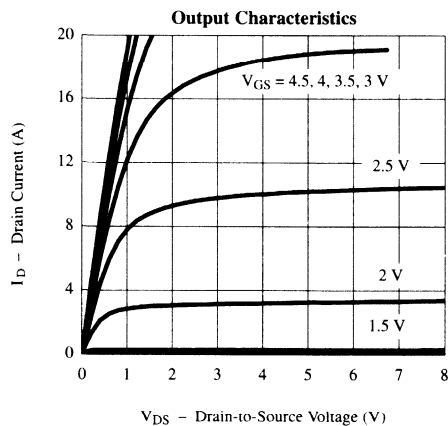
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	15			A
		$V_{DS} \geq 5\ \text{V}, V_{GS} = 3.0\ \text{V}$	6			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 3.3\ \text{A}$		0.048	0.075	Ω
		$V_{GS} = 3.0\ \text{V}, I_D = 2.7\ \text{A}$		0.067	0.110	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 3.3\ \text{A}$		10.3		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.25\ \text{A}, V_{GS} = 0\ \text{V}$		0.7	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 6\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 0.3\ \text{A}$		4.5	9.0	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			0.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\ \text{V}, R_L = 20\ \Omega$ $I_D = 0.3\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		8	20	ns
Rise Time	t_r			6	15	
Turn-Off Delay Time	$t_{d(off)}$			12	25	
Fall Time	t_f			16	30	
Source-Drain Reverse Recovery Time	t_{rr}			52	80	

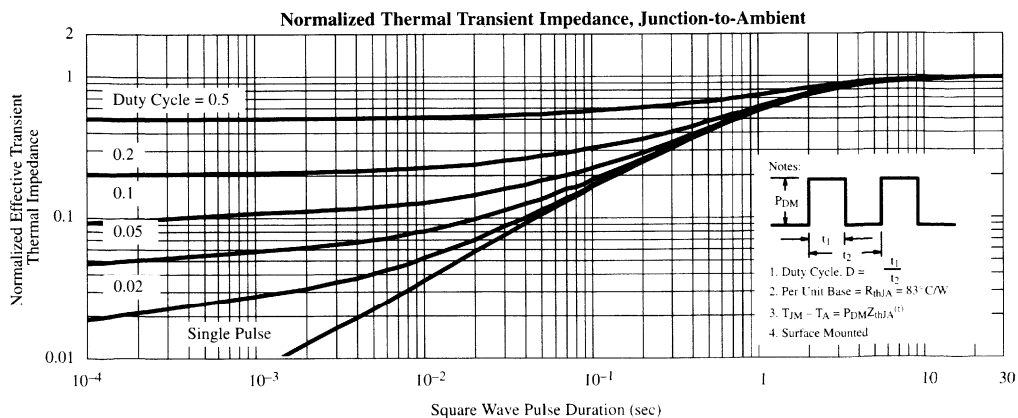
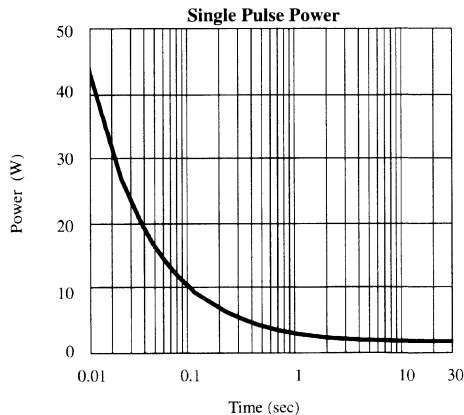
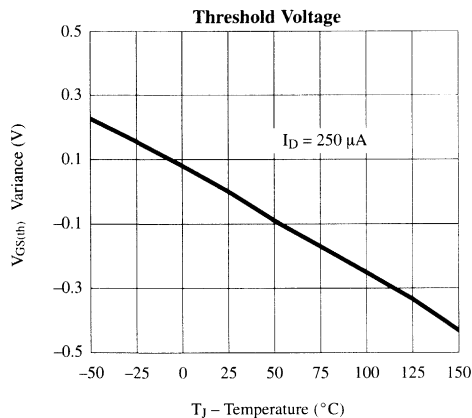
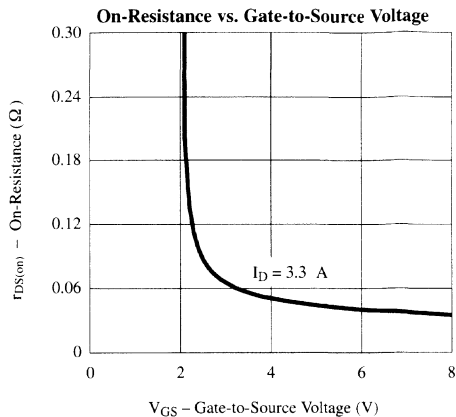
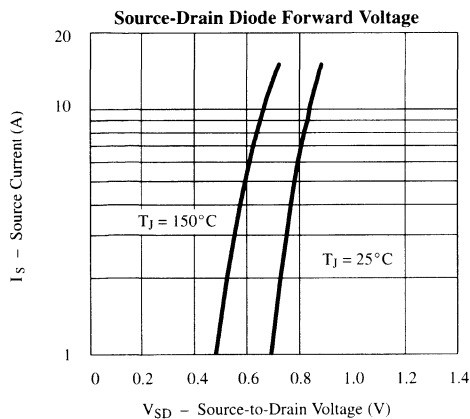
Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

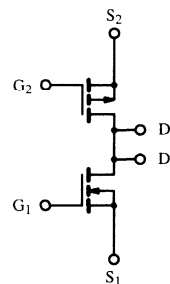
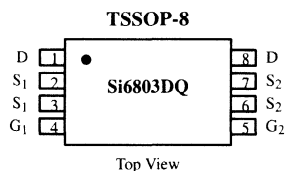


N-/P-Ch Half-Bridge, Reduced Q_g , Fast Switching MOSFET

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.095 @ $V_{GS} = 4.5$ V	± 2.5
		0.145 @ $V_{GS} = 3.0$ V	± 2.0
P-Channel	-20	0.110 @ $V_{GS} = -4.5$ V	± 2.3
		0.165 @ $V_{GS} = -3.0$ V	± 1.9

High-Efficiency
PWM Optimized



N-Channel MOSFET

4

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current ($T_J = 150^{\circ}\text{C}$) ^a	$T_A = 25^{\circ}\text{C}$	I_D	± 2.5	± 2.3	A
	$T_A = 70^{\circ}\text{C}$		± 2.0	± 1.9	
Pulsed Drain Current		I_{DM}	± 10		
Continuous Source Current (Diode Conduction) ^a		I_S	1.0	-1.0	
Maximum Power Dissipation ^a	$T_A = 25^{\circ}\text{C}$	P_D	1.0		W
	$T_A = 70^{\circ}\text{C}$		0.64		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	N-Ch	0.6		V
		$V_{DS} = V_{GS}, I_D = -250\ \mu A$	P-Ch	-0.6		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V, V_{GS} = \pm 12\ V$	N-Ch P-Ch		± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ V, V_{GS} = 0\ V$	N-Ch		1	μA
		$V_{DS} = -20\ V, V_{GS} = 0\ V$	P-Ch		-1	
		$V_{DS} = 20\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	N-Ch		25	
		$V_{DS} = -20\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	P-Ch		-25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ V, V_{GS} = 4.5\ V$	N-Ch	10		A
		$V_{DS} = -5\ V, V_{GS} = -4.5\ V$	P-Ch	-10		
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ V, I_D = 2.5\ A$	N-Ch		0.076	Ω
		$V_{GS} = -4.5\ V, I_D = 2.3\ A$	P-Ch		0.086	
		$V_{GS} = 3.0\ V, I_D = 2.0\ A$	N-Ch		0.105	
		$V_{GS} = -3.0\ V, I_D = 1.9\ A$	P-Ch		0.122	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ V, I_D = 2.5\ A$	N-Ch		5.5	S
		$V_{DS} = -15\ V, I_D = -2.3\ A$	P-Ch		6.0	
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.0\ A, V_{GS} = 0\ V$	N-Ch		0.75	V
		$I_S = -1.0\ A, V_{GS} = 0\ V$	P-Ch		0.75	
Dynamic ^a						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 3.5\ V, V_{GS} = 4.5\ V, I_D = 0.3\ A$ P-Channel $V_{DS} = -3.5\ V, V_{GS} = -4.5\ V$ $I_D = -0.3\ A$	N-Ch		3.8	nC
Gate-Source Charge	Q_{gs}		P-Ch		5.2	
			N-Ch		0.8	
Gate-Drain Charge	Q_{gd}		P-Ch		1.3	
Turn-On Delay Time	$t_{d(on)}$	N-Ch		0.3		
		P-Ch		0.6		
Rise Time	t_r	N-Ch		14	30	
		P-Ch		12		
Turn-Off Delay Time	$t_{d(off)}$	N-Ch		34	70	
		P-Ch		32		
Fall Time	t_f	N-Ch		25	50	
		P-Ch		22		
Source-Drain Reverse Recovery Time	t_{rr}	N-Ch		10	25	
		P-Ch		12		
		N-Ch		50	80	
		P-Ch		50		

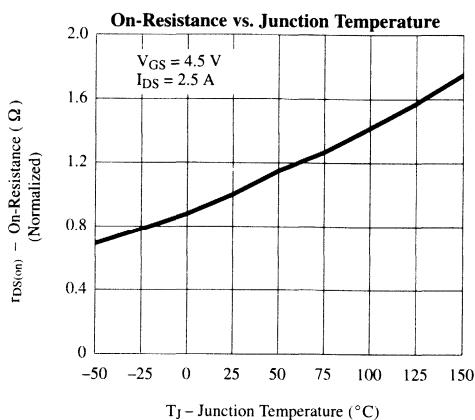
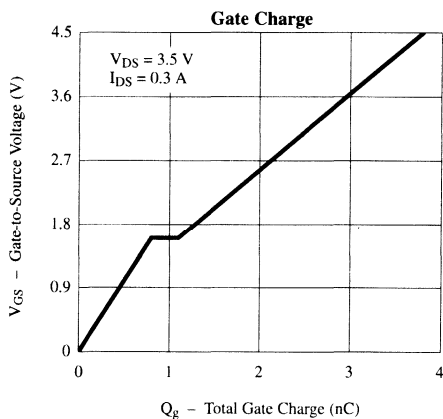
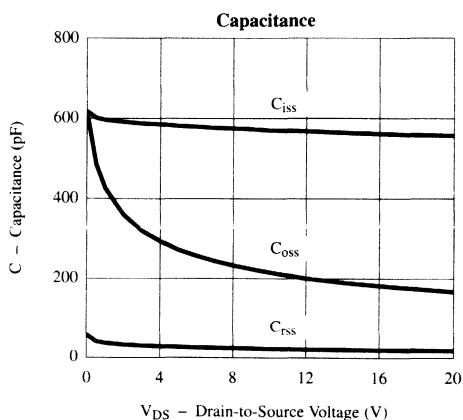
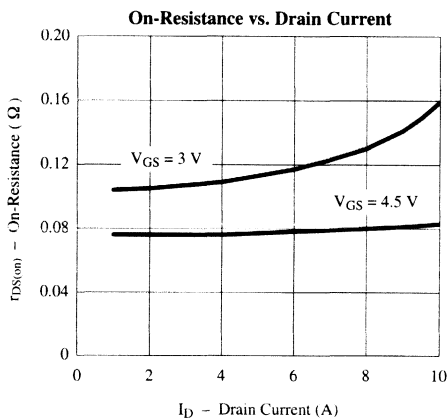
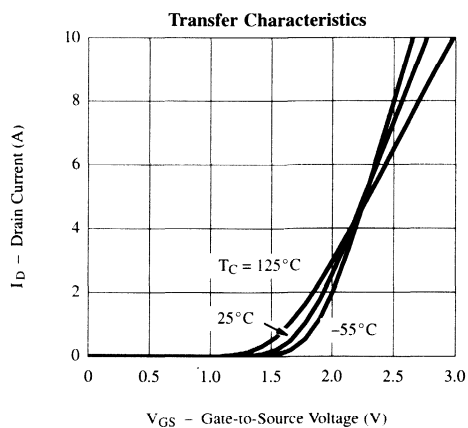
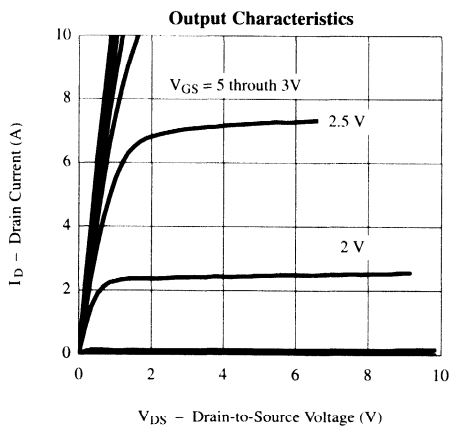
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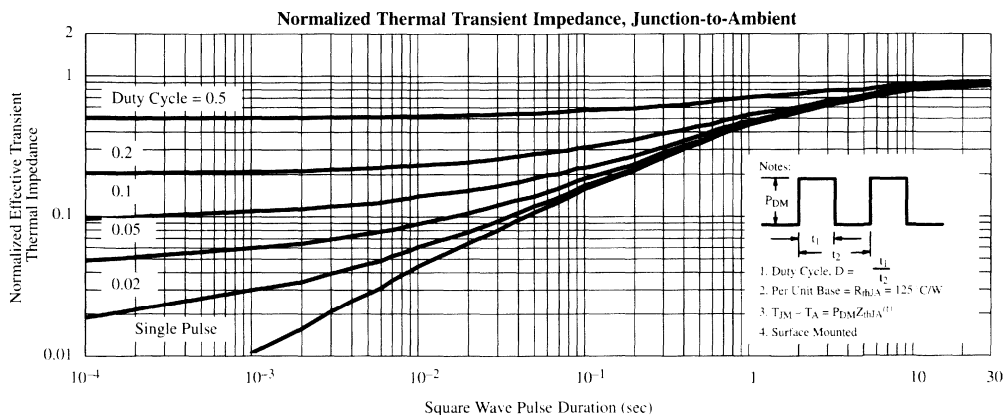
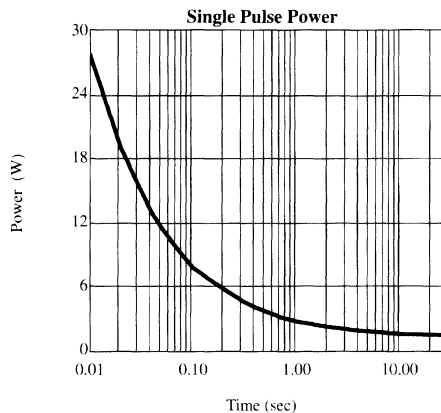
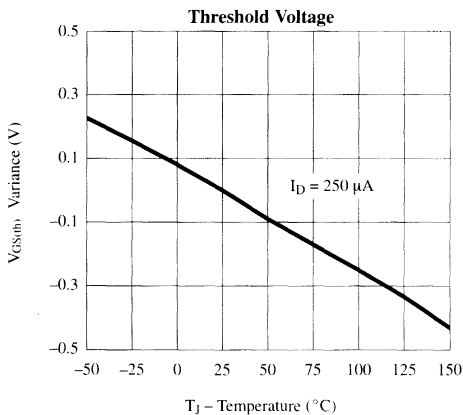
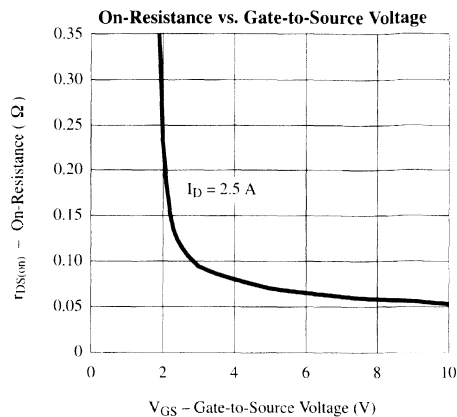
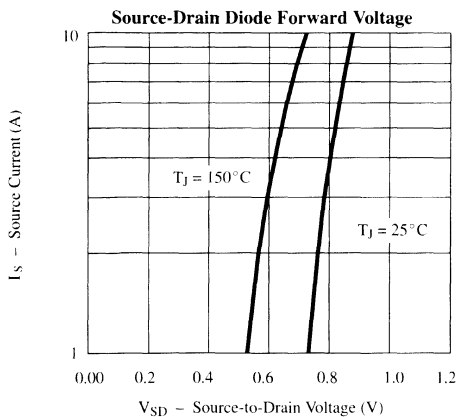
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Noted)

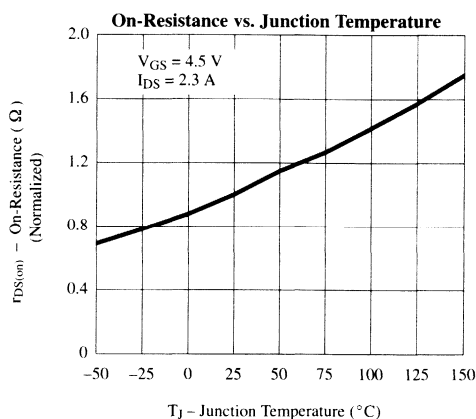
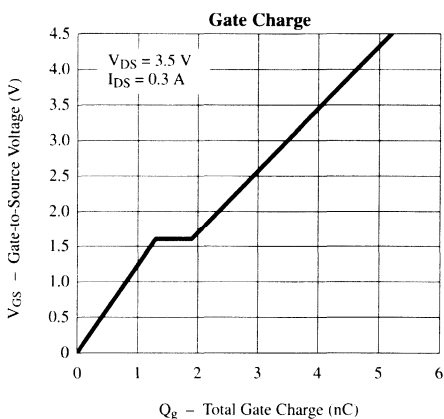
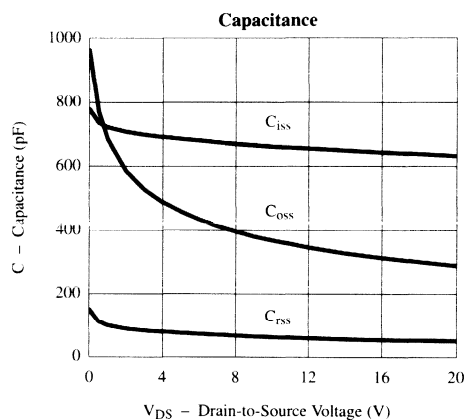
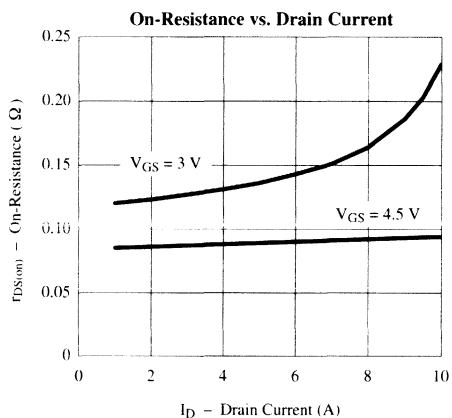
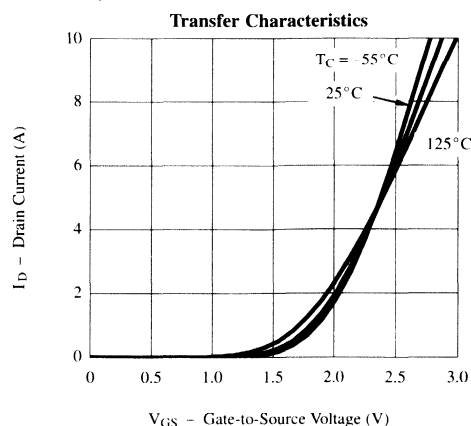
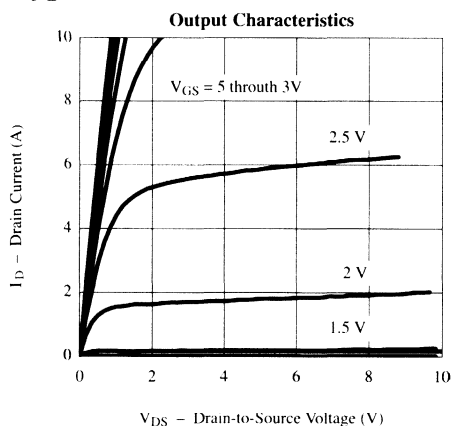
N-Channel



Typical Characteristics (25°C Unless Noted)
N-Channel


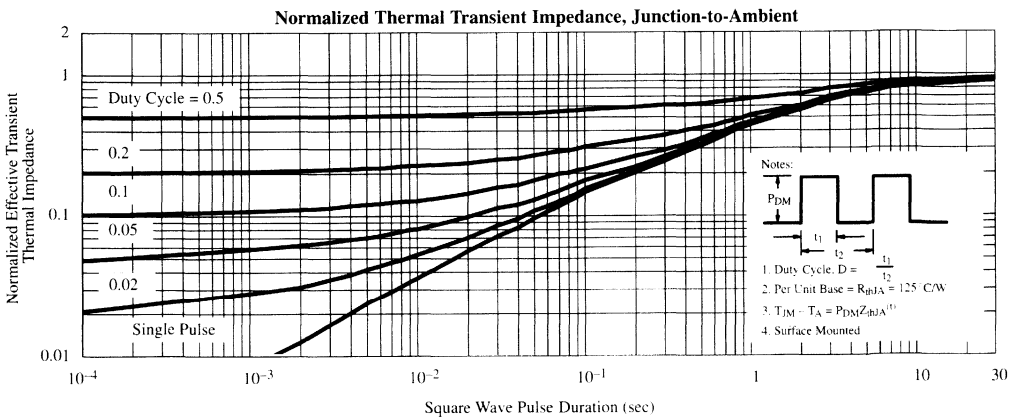
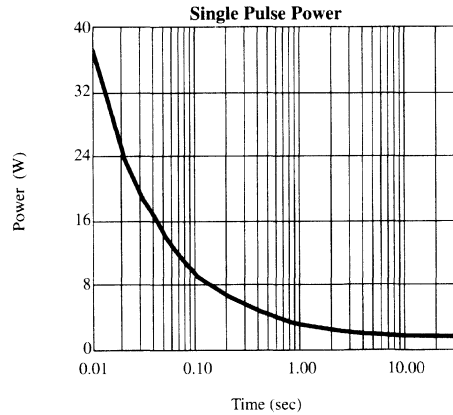
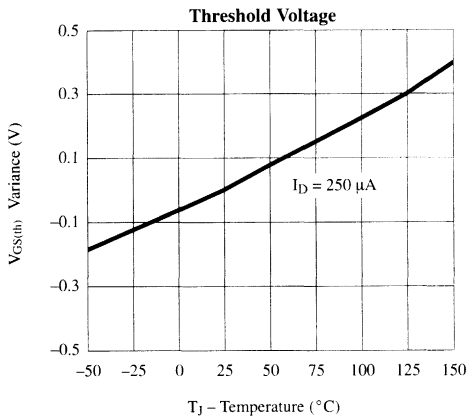
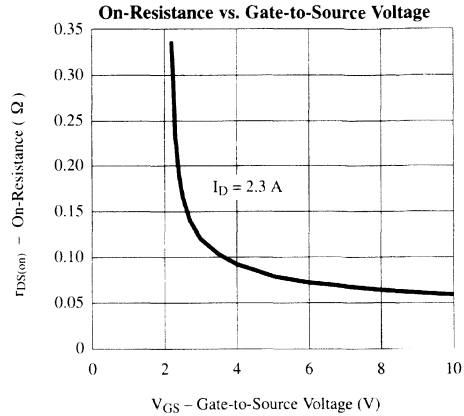
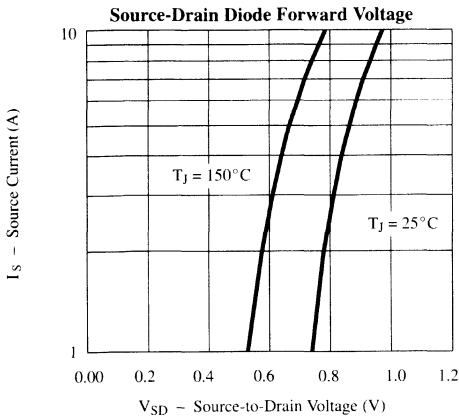
Typical Characteristics (25°C Unless Noted)

P-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

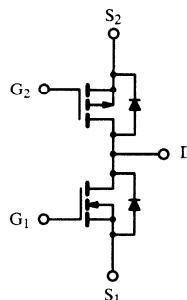
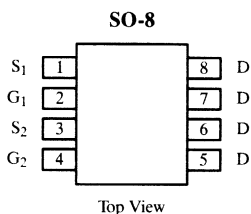


Dual N- and P-Channel, Reduced Q_g , Fast Switching Half-Bridge

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.055 @ $V_{GS} = 4.5$ V	± 4.5
		0.075 @ $V_{GS} = 3.0$ V	± 3.8
P-Channel	-20	0.080 @ $V_{GS} = -4.5$ V	± 4.0
		0.120 @ $V_{GS} = -3.0$ V	± 3.0

High-Efficiency
PWM Optimized



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	−20	V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 4.5	± 4.0	A
	T _A = 70°C		± 3.6	± 3.0	
Pulsed Drain Current		I _{DM}	± 20		
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	−1.7	W
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.0		
	T _A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70712.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

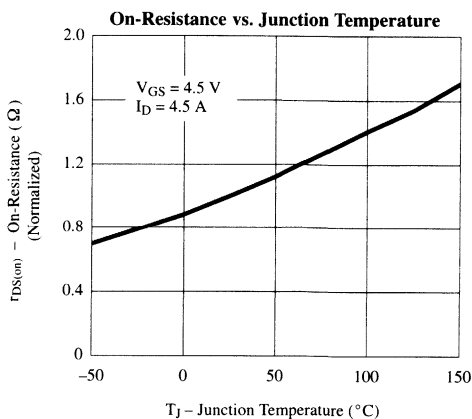
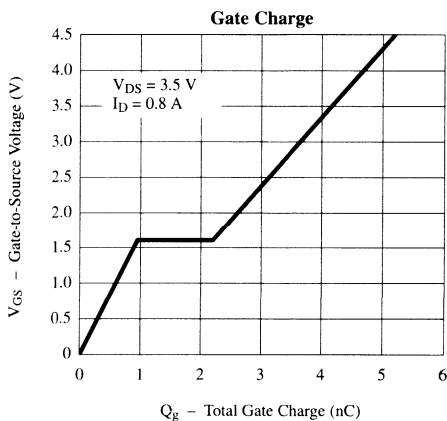
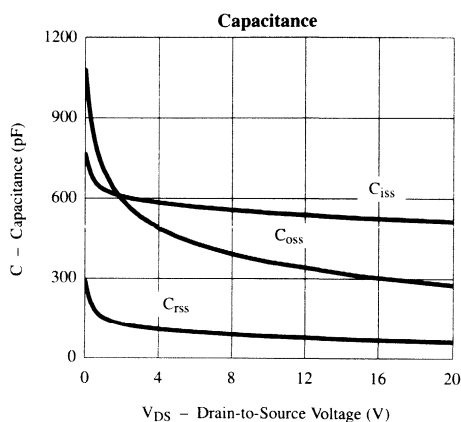
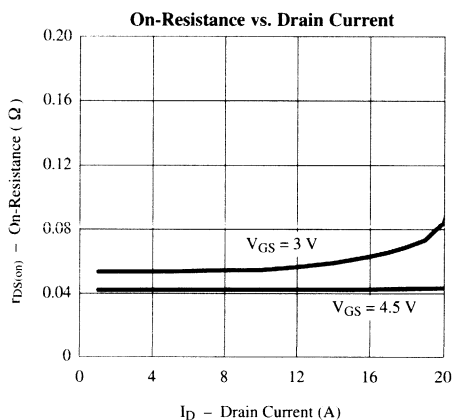
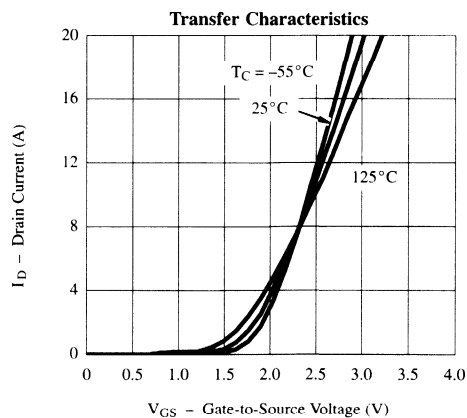
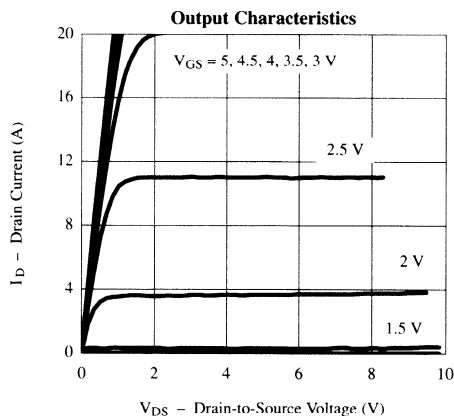
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	N-Ch	0.6		V	
		$V_{DS} = V_{GS}, I_D = -250\ \mu A$	P-Ch	-0.6			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V, V_{GS} = \pm 12\ V$	N-Ch P-Ch		± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ V, V_{GS} = 0\ V$	N-Ch		1	μA	
		$V_{DS} = -20\ V, V_{GS} = 0\ V$	P-Ch		-1		
		$V_{DS} = 20\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	N-Ch		25		
		$V_{DS} = -20\ V, V_{GS} = 0\ V, T_J = 70^\circ C$	P-Ch		-25		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ V, V_{GS} = 4.5\ V$	N-Ch	20		A	
		$V_{DS} = -5\ V, V_{GS} = -4.5\ V$	P-Ch	-20			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ V, I_D = 4.5\ A$	N-Ch		0.044	0.055	Ω
		$V_{GS} = -4.5\ V, I_D = 4.0\ A$	P-Ch		0.064	0.080	
		$V_{GS} = 3.0\ V, I_D = 3.8\ A$	N-Ch		0.055	0.075	
		$V_{GS} = -3.0\ V, I_D = 3.0\ A$	P-Ch		0.086	0.120	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ V, I_D = 4.5\ A$	N-Ch		11.5	S	
		$V_{DS} = -15\ V, I_D = -4.0\ A$	P-Ch		9.8		
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\ A, V_{GS} = 0\ V$	N-Ch		0.73	1.2	V
		$I_S = -1.7\ A, V_{GS} = 0\ V$	P-Ch		-0.75	-1.2	
Dynamic ^a							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 3.5\ V, V_{GS} = 4.5\ V, I_D = 0.8\ A$ P-Channel $V_{DS} = -3.5\ V, V_{GS} = -4.5\ V$ $I_D = -0.8\ A$	N-Ch		5.2	10	nC
Gate-Source Charge	Q_{gs}		P-Ch		7.9	15	
			N-Ch		0.95		
Gate-Drain Charge	Q_{gd}		P-Ch		1.60		
		N-Ch		1.15			
Turn-On Delay Time	$t_{d(on)}$	P-Ch		1.90			
		N-Ch		12	20	ns	
Rise Time	t_r	P-Ch		20	40		
		N-Ch		22	50		
Turn-Off Delay Time	$t_{d(off)}$	P-Ch		52	90		
		N-Ch		27	50		
Fall Time	t_f	P-Ch		37	60		
		N-Ch		8	20		
Source-Drain Reverse Recovery Time	t_{rr}	P-Ch		11	20		
		N-Channel— $I_F = 1.7\ A, di/dt = 100\ A/\mu s$ P-Channel— $I_F = -1.7\ A, di/dt = 100\ A/\mu s$	N-Ch P-Ch		60 60	100 100	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

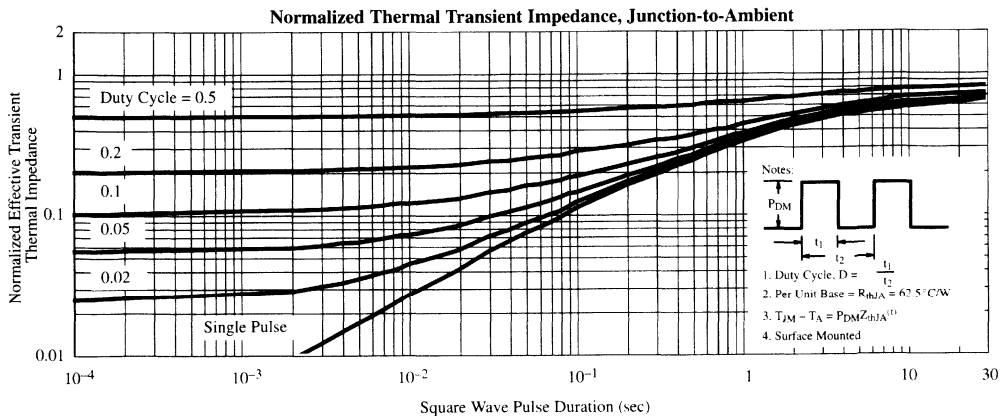
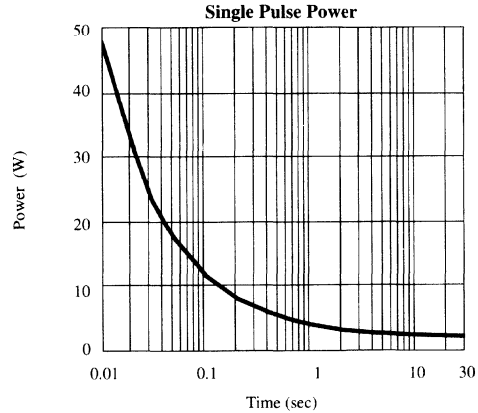
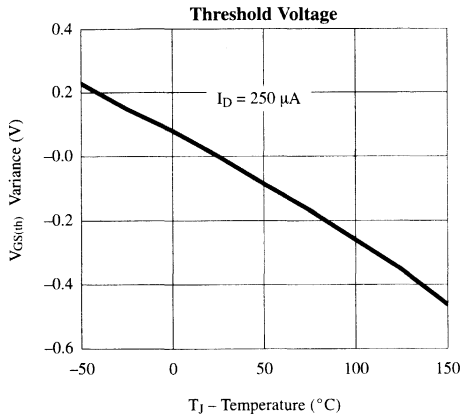
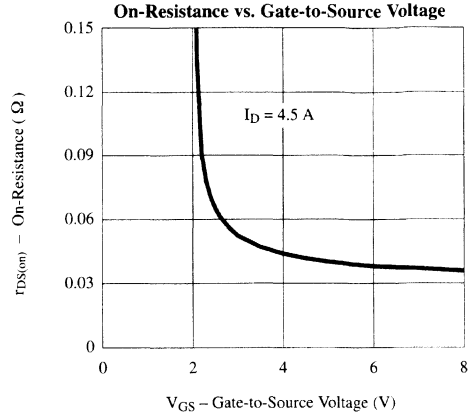
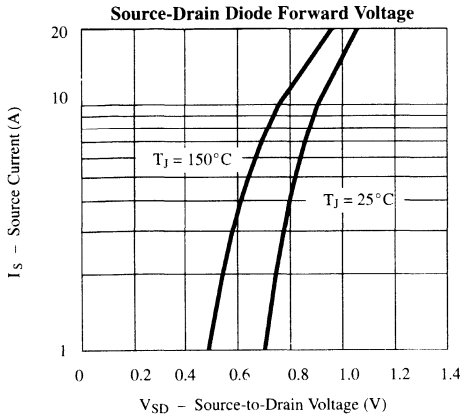
Typical Characteristics (25°C Unless Noted)

N-Channel



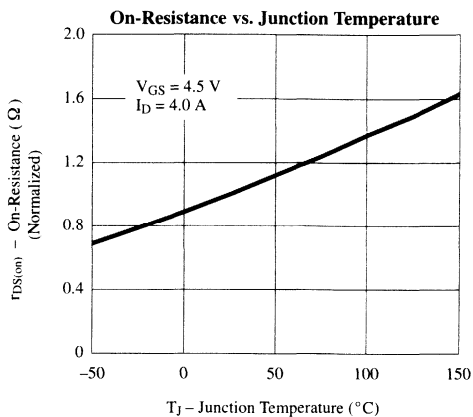
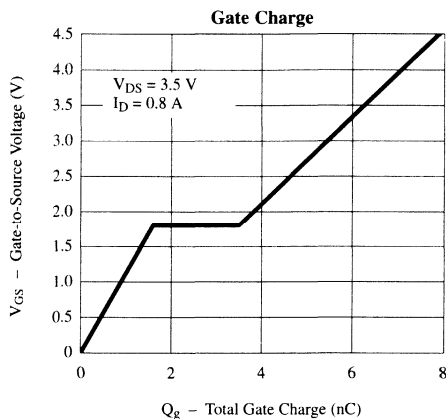
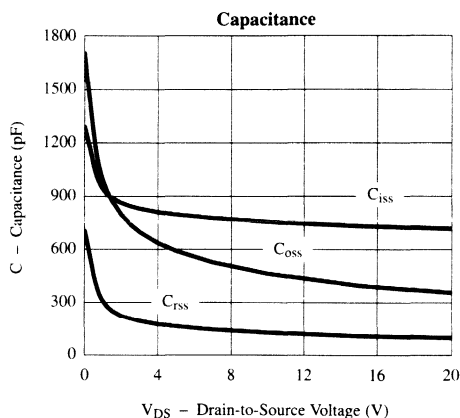
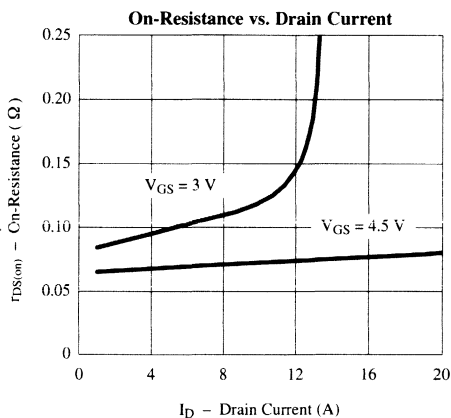
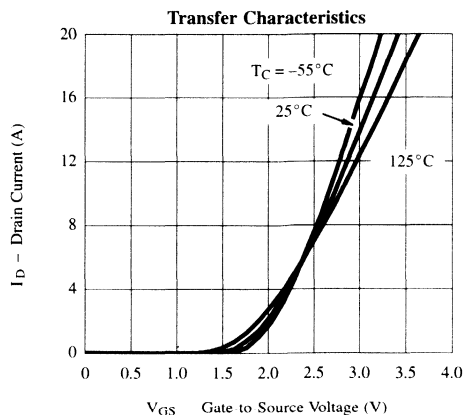
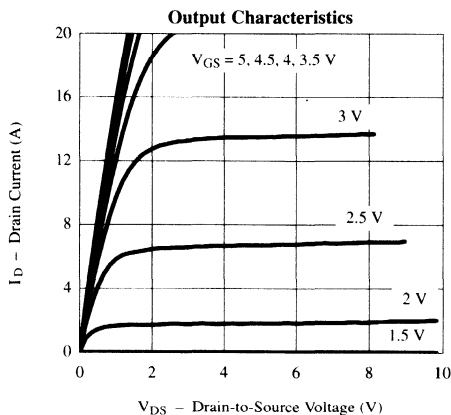
Typical Characteristics (25°C Unless Noted)

N-Channel



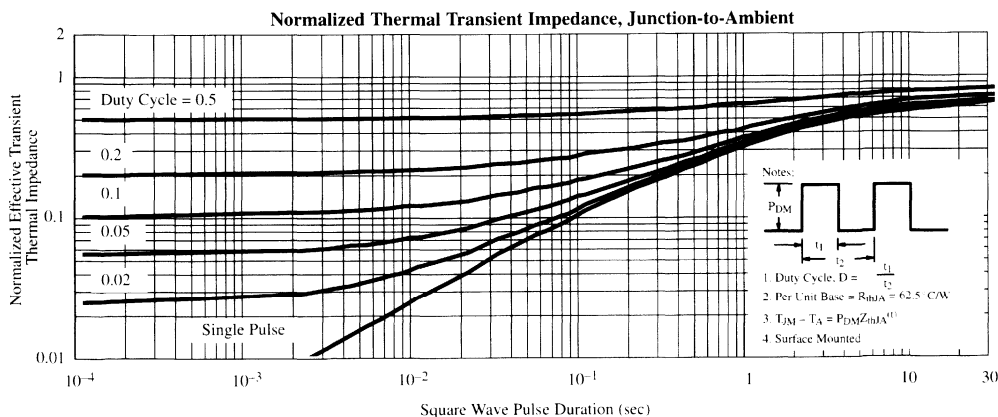
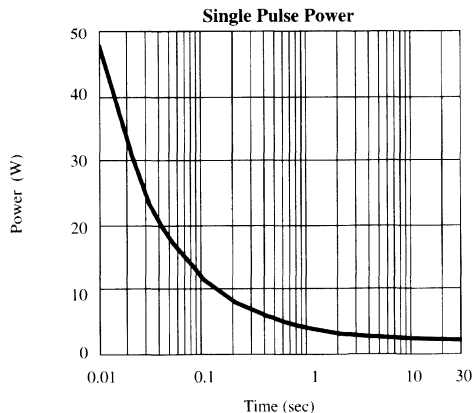
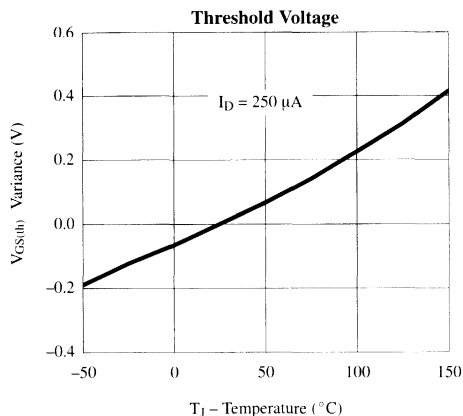
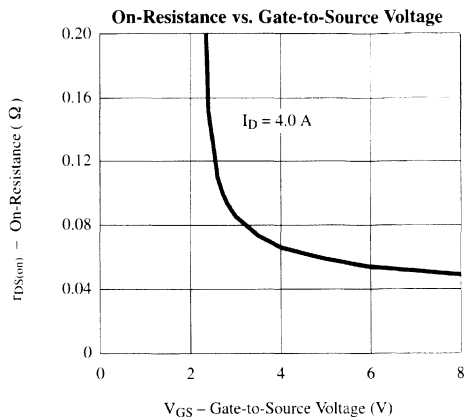
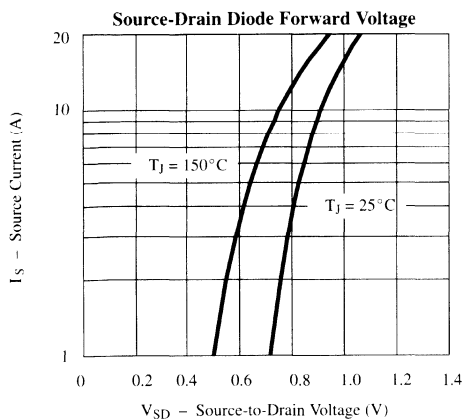
Typical Characteristics (25°C Unless Noted)

P-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

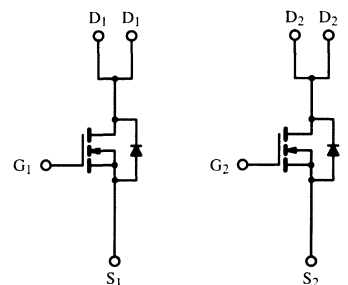
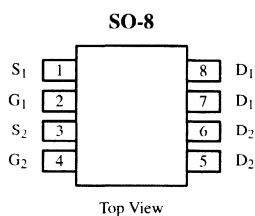


Dual N-Channel Reduced Q_g , Fast Switching MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.055 @ $V_{GS} = 4.5$ V	± 4.5
	0.075 @ $V_{GS} = 3.0$ V	± 3.8

High-Efficiency
PWM Optimized



N-Channel MOSFET

N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$ ± 4.5	A
		$T_A = 70^\circ\text{C}$ ± 3.6	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 25	
Continuous Source Current (Diode Conduction) ^a	I_S	± 1.7	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$ 2	W
		$T_A = 70^\circ\text{C}$ 1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70625.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

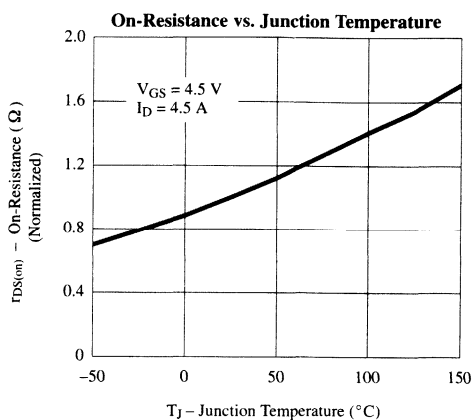
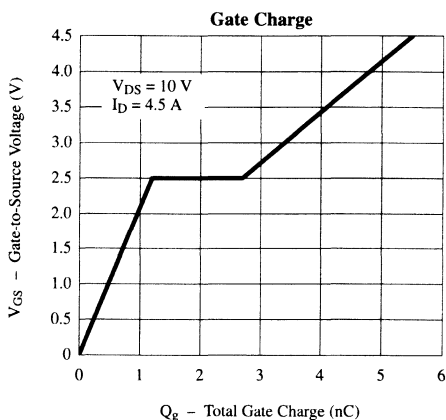
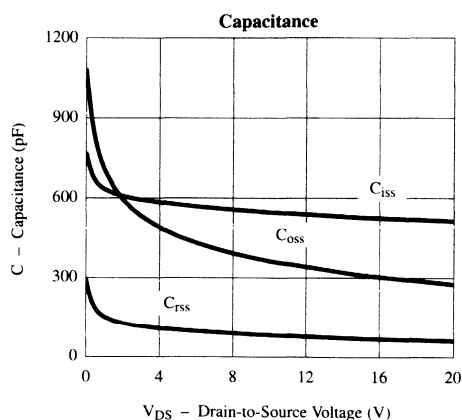
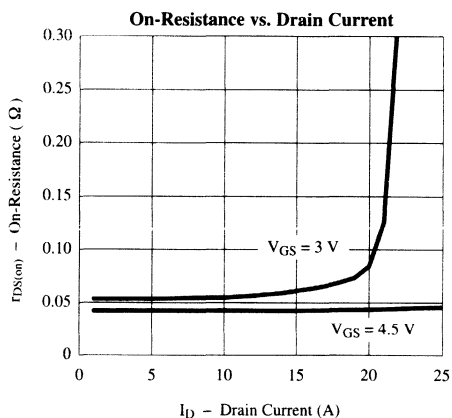
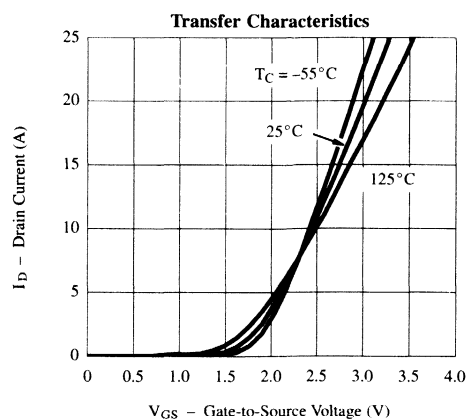
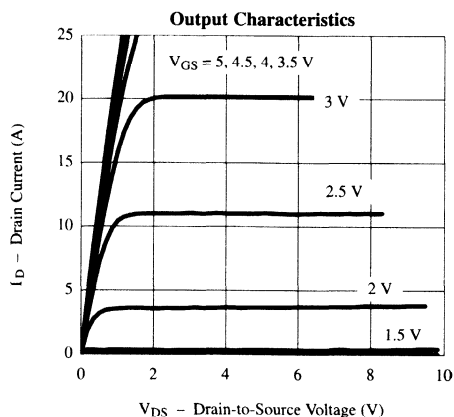
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 5\ \text{V}$	25			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 4.5\ \text{A}$		0.044	0.055	Ω
		$V_{GS} = 3.0\ \text{V}, I_D = 3.8\ \text{A}$		0.055	0.075	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 4.5\ \text{A}$		11.5		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$		0.73	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 4.5\ \text{A}$		5.5	10	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D = 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		12	25	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			23	50	
Fall Time	t_f			9	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	100	

Notes

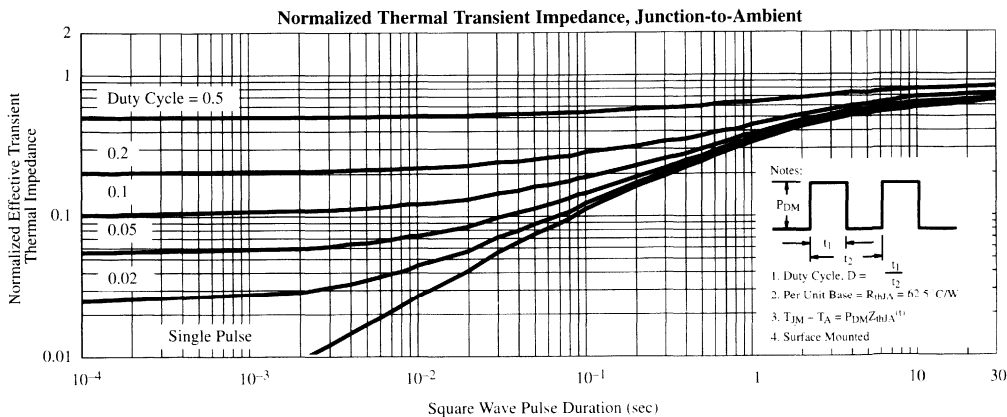
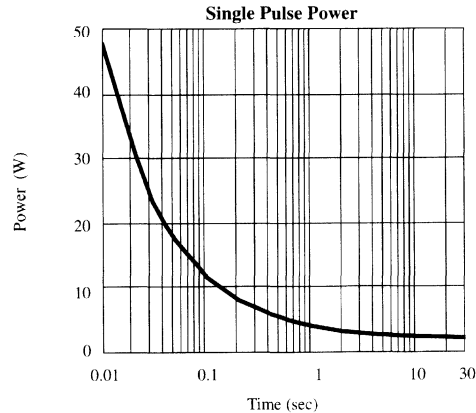
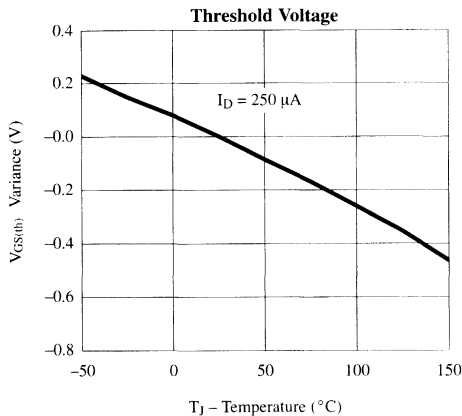
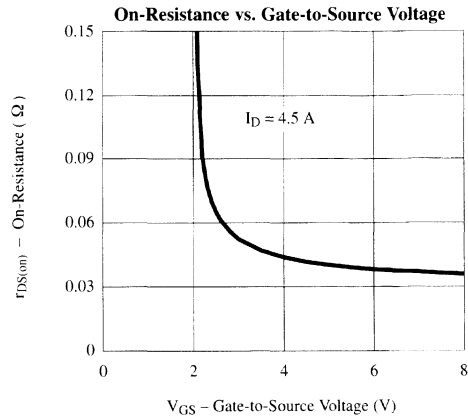
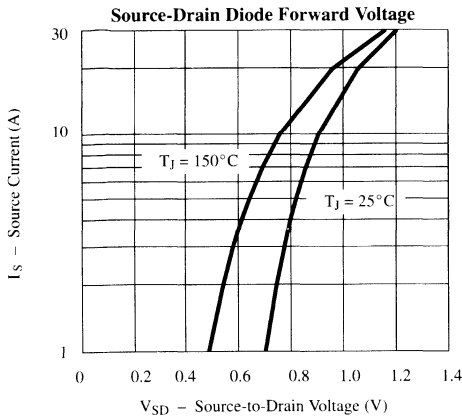
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

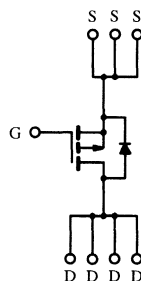
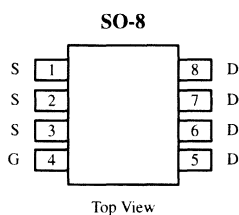


P-Channel Reduced Q_g , Fast Switching MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-25	0.040 @ $V_{GS} = -4.5$ V	± 5.9
	0.060 @ $V_{GS} = -3.0$ V	± 4.8

High-Efficiency
PWM Optimized



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-25	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 5.9	A
		± 4.7	
Pulsed Drain Current	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	W
Maximum Power Dissipation ^a	P_D	2.5	
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

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Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

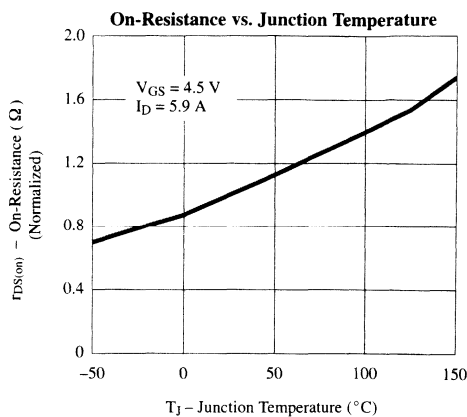
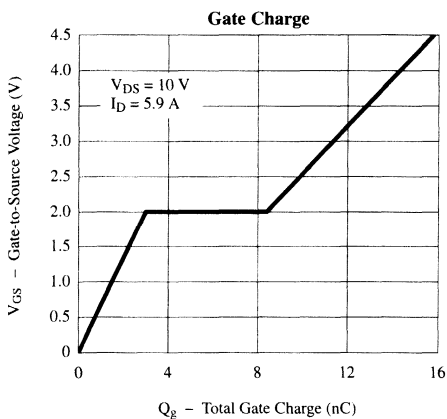
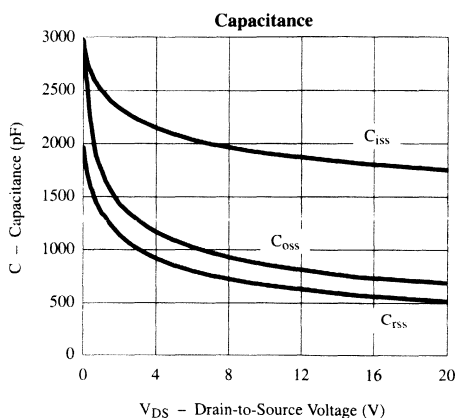
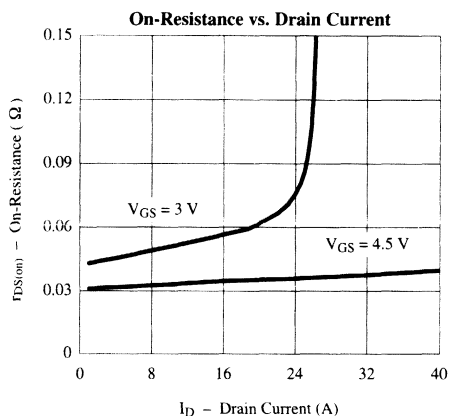
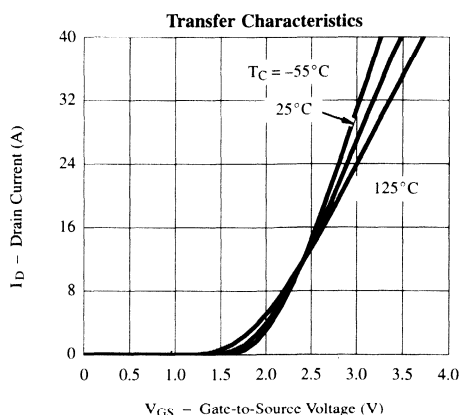
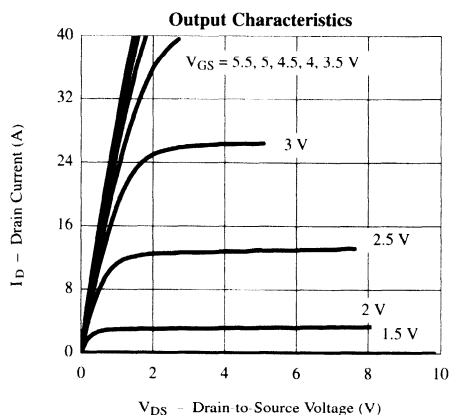
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -25\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -25\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-40			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -5.9\ \text{A}$		0.033	0.040	Ω
		$V_{GS} = -3.0\ \text{V}, I_D = -2.0\ \text{A}$		0.044	0.060	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -9\ \text{V}, I_D = -5.9\ \text{A}$		18		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.1\ \text{A}, V_{GS} = 0\ \text{V}$		-0.75	-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -5.9\ \text{A}$		15.8	25	nC
Gate-Source Charge	Q_{gs}			3.0		
Gate-Drain Charge	Q_{gd}			5.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		20	40	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			53	100	
Fall Time	t_f			31	60	
Source-Drain Reverse Recovery Time	t_{rr}			80	120	

Notes

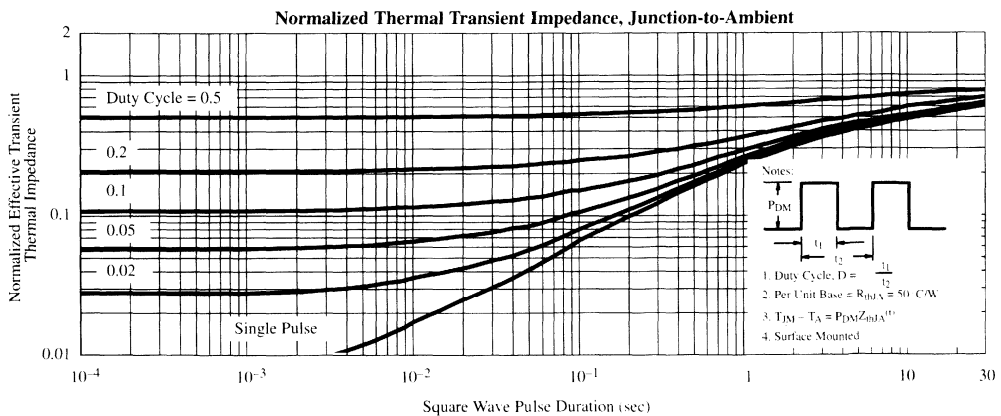
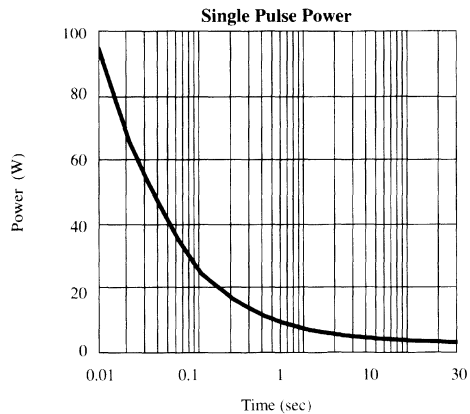
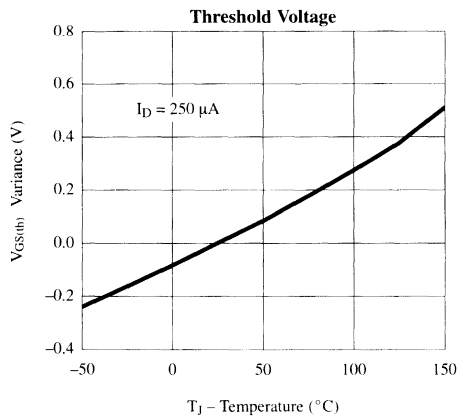
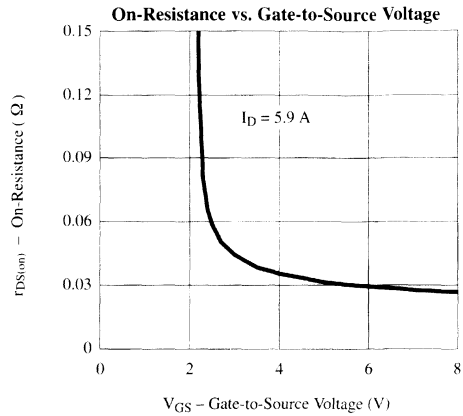
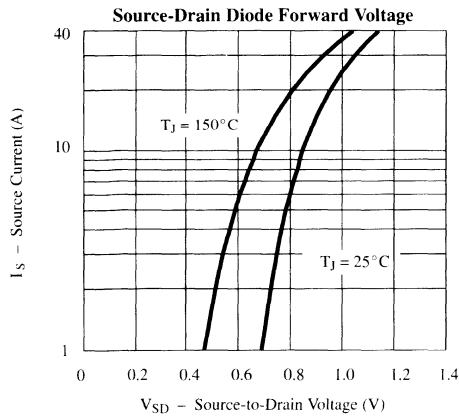
a. For design aid only; not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

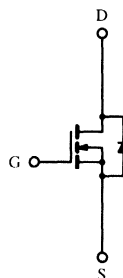
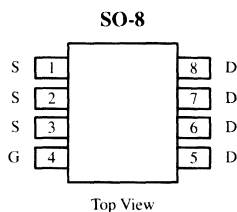


N-Channel Reduced Q_g , Fast Switching MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
25	0.023 @ $V_{GS} = 4.5$ V	± 7.8
	0.030 @ $V_{GS} = 3.0$ V	± 6.8

High-Efficiency
PWM Optimized



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 7.8	A
		± 6.2	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	± 2.1	
Maximum Power Dissipation ^a	P_D	2.5	W
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

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Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

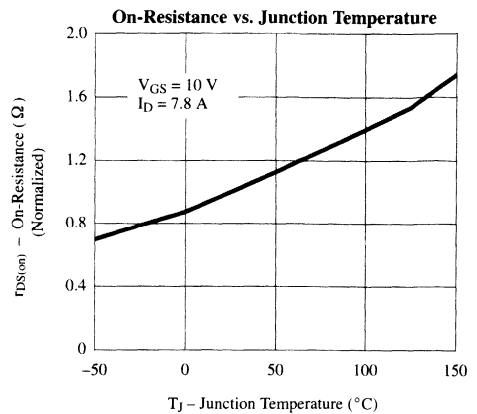
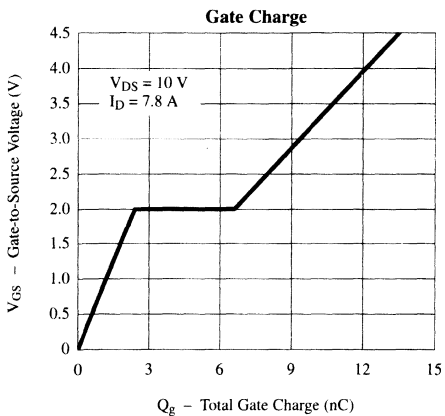
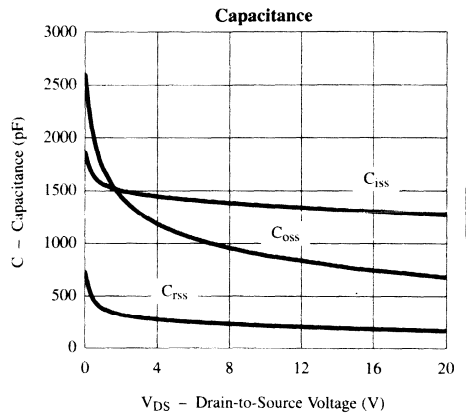
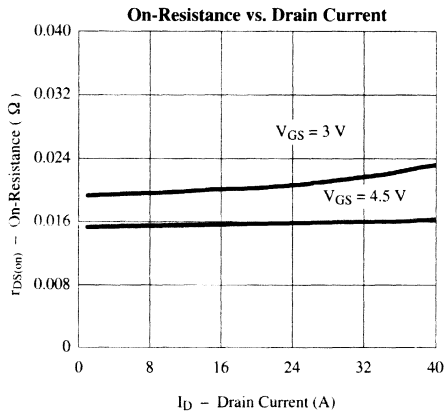
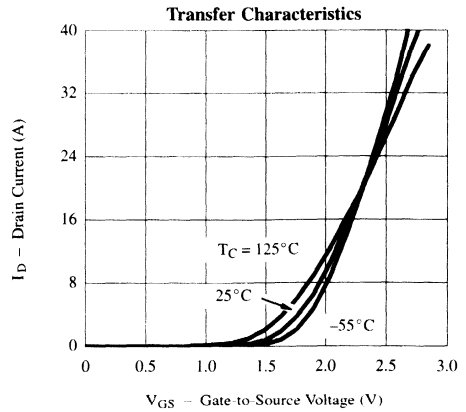
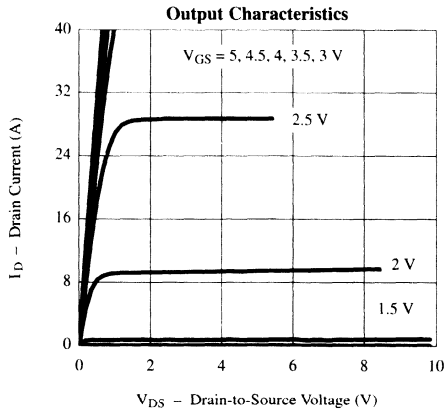
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	40			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 7.8\ \text{A}$		0.018	0.023	Ω
		$V_{GS} = 3.0\ \text{V}, I_D = 6.8\ \text{A}$		0.022	0.030	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 7.8\ \text{A}$		25		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\ \text{A}, V_{GS} = 0\ \text{V}$		0.71	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 7.8\ \text{A}$		13.5	20	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			4.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			46	90	
Fall Time	t_f			18	35	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		80	120	

Notes

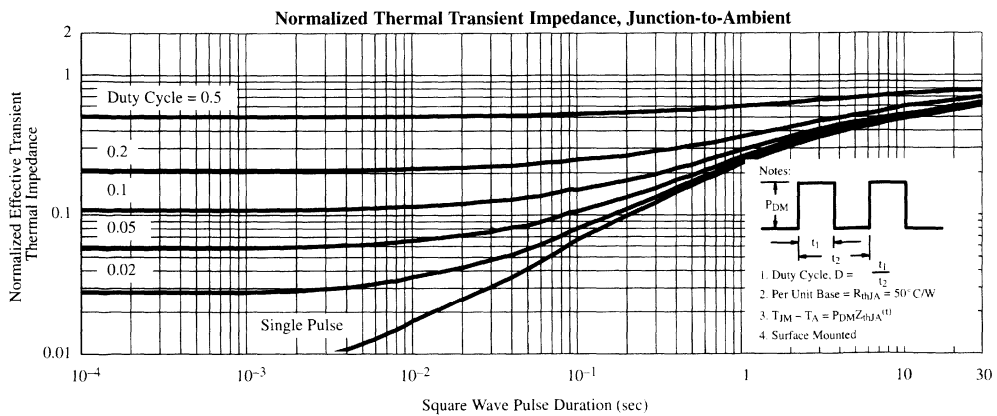
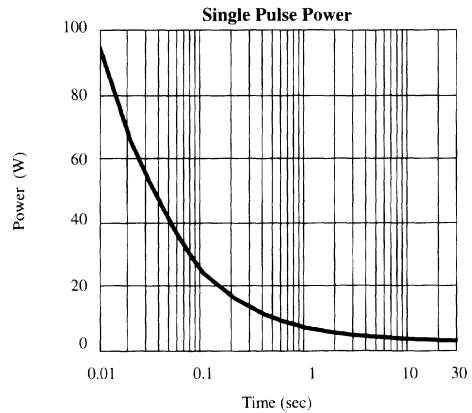
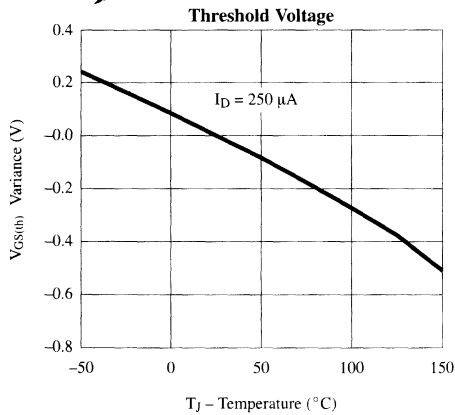
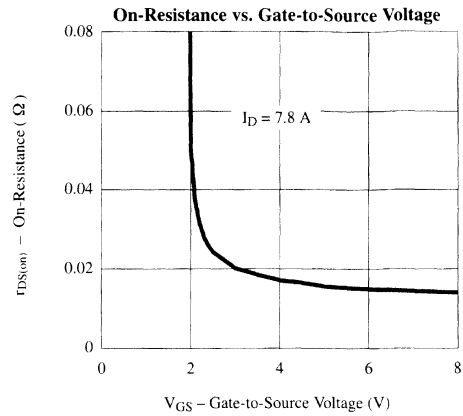
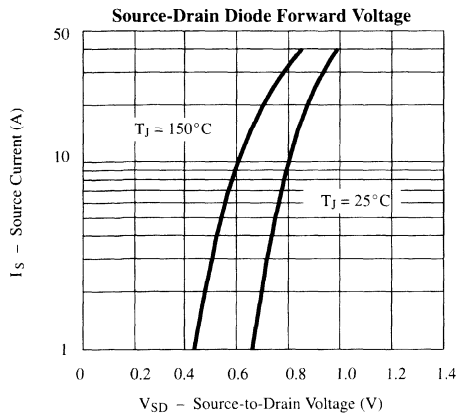
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)



Mathematical Symbols and Abbreviations

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Application Notes for Siliconix Power Products

Application Note Number	FaxBack Number	Description
LITTLE FOOT® MOSFETs		
AN801	70591	Designing with Complementary Power MOSFETs in Surface-Mount (SO-8) Packages The LITTLE FOOT complementary n- and p-channel Si9942DY can be used to drive inductive loads such as motors, solenoids, and relays directly, or it may be used as a low-impedance buffer to drive larger power MOSFETs or capacitive loads. In 12-V battery-powered applications, the Si9942DY allows a substantial increase in motor size without the need for additional heatsinking.
AN802	70592	Low-Voltage Motor Drive Designs Using N-Channel Dual MOSFETs in Surface-Mount Packages Dual n-channel LITTLE FOOT devices offer on-resistance advantages which extend the power range of surface-mount power devices. With the selection of a high-side gate drive circuit that complements an application's needs, an n-channel half-bridge can provide a surface-mount option that is economical and reliable.
AN803	70593	Thermal Characteristics of Siliconix's LITTLE FOOT Family of Surface-Mount MOSFETs Siliconix' LITTLE FOOT family of surface-mount power MOSFETs provides improved thermal transfer characteristics, high current handling capability, and lower on-resistance compared with DPAK and SOT packages. The copper lead frames designed for the LITTLE FOOT family maximize heat transfer to the PC board. Combined with Siliconix' high-density transistor technologies, the result is a significantly extended range for surface-mount devices in power applications.
AN805	70649	Power MOSFETs Optimized for Low-Voltage DC/DC Conversion Designers of low-voltage dc-to-dc converters have two main concerns: reducing size and reducing losses. As a way of reducing size, designers are increasing switching frequencies. But the result has often been reduced converter efficiency. To minimize losses, MOSFET manufacturers have generally focused on lowering on-resistance. But the results have not been optimal for dc-to-dc conversion designs, since gate charge and switching speed issues have been largely ignored. The dominant losses associated with MOSFETs were once conduction losses, but this is no longer the case.
AN806	70738	Mounting LITTLE FOOT TSSOP-8 Power MOSFETs Recommended electrical connections and pad patterns for the LITTLE FOOT TSSOP-8.
AN807	70739	Mounting LITTLE FOOT SOT-23 Power MOSFETs Recommended electrical connections, footprints, and soldering procedures for the LITTLE FOOT SOT-23.
AN808	70740	Mounting LITTLE FOOT SO-8 Power MOSFETs Recommended electrical connections and pad patterns for the LITTLE FOOT SO-8.
AN809	70741	Mounting LITTLE FOOT TSOP-6 Power MOSFETs Recommended electrical connections, footprints, and soldering procedures for the LITTLE FOOT TSOP-6.
AN1001	70571	The Next Step in Surface-Mount Power MOSFETs The next step in surface-mount power MOSFETs combines high-density n- and p-channel technologies with TSSOP packaging. With a 1.1 mm profile, these devices are small enough to fit into any standard PC Card (PCMCIA) card. They provide an equally compact solution for load switching in small form-factor disk drives, cellular telephones, notebook computers, PDAs, and other applications where space and battery life is at a premium.

Application Notes for Siliconix Power Products (Cont'd)

Application Note Number	FaxBack Number	Description
Power MOSFETs		
AN601	70572	Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments This application note reviews the history of unclamped inductive switching (UIS) and examines various theories pertaining to failure. It further identifies what appears to be two related mechanisms -- thermal and bipolar -- believed to be responsible for failure during UIS and concludes by recommending how a power MOSFET should be qualified for ruggedness in the data sheet.
AN603	70573	Designing With the Si9978DW Configurable H-Bridge Controller The Si9978DW monolithic controller confronts issues common to bipolar and MOS technology parts. Separating the controller from the MOSFETs assures flexible current handling, small size and ease of assembly. The Si9978DW is designed to be used with LITTLE FOOT MOSFETs to create an all-n-channel H-bridge or two separate half bridges. The dual function allows flexibility, standardization of components and reduced inventory costs. Features are an integral high-side drive circuitry and an internal voltage regulator, which allows operation over a 20- to 40-V dc input voltage range. Protection features include cross-conduction protection and current limiting. The FAULT outputs indicate undervoltage lockout or overcurrent shutdown.
AN604	70654	Si9993 — Hard Disk Drive Combination Spindle and VCM Controller The Si9993 is a combination spindle motor and VCM (voice coil motor) controller which combines, in a single package, all of the sensorless commutation, pulse-width modulation (PWM), braking, and FET drive circuitry for a hard disk drive spindle motor.
AN901	70612	Depletion-Mode MOSFETs Expand Circuit Opportunities A principal advantage of the depletion-mode MOSFET is its ability to perform at high operating voltage than its JFET counterpart. With the introduction of the ND2012 and ND2406 series, with BV > 200 V and > 240 V respectively, sensitivity to ESD has been reduced greatly.
Power ICs		
AN701	70575	Designing High-Frequency DC-to-DC Converters with the Si9114 Switchmode Controller The Si9114 controller enables high-frequency power conversion by reducing delay times and adding additional features over previous generation products. As a result, dc-to-dc converters can be designed for frequencies up to 1 MHz with simple PWM topologies instead of the complex resonant ones. High-frequency designs with the Si9114 will enable designers to reduce the size of energy storage components, increase reliability by using ceramic capacitors, and simplify the implementation of a distributed power architecture.
AN702	70576	Efficient ISDN Power Converters Using the Si9100 The Si9100 power IC facilitates compliance with ISDN design requirements with a minimum number of external parts. To illustrate this capability, a discontinuous conduction mode (DCM) flyback converter was built and tested with measured efficiency greater than 80% for a wide range of loads.
AN703	70577	Designing DC/DC Converters with the Si9110 Switchmode Controller Si9110 is the first BiC/DMOS switchmode controller IC to provide switching frequencies in the 100- to 500-kHz range while keeping current limit delay time under approximately 100 ns. To illustrate the Si9110's capabilities, a 15-W forward converter is presented, providing 5-V and 12-V outputs from a 9- to 36-V input range.
AN704	70578	Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals This application note specifically addresses design issues relating to emergency-designated ISDN terminals and presents design details for a dc-to-dc converter which conforms to the international standard.
AN705	70579	The Si9910DY Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications The Si9910DY introduces a new generation of "adaptive" power MOSFET gate drivers that use active feedback to protect the power MOSFET, while allowing logic-level control of high-voltage signals. When all of its protective options are enabled, the Si9910DY is capable of controlling the power MOSFET dv/dt, maximum peak current, minimum gate-drive voltage, and maximum source-drain voltage drop.

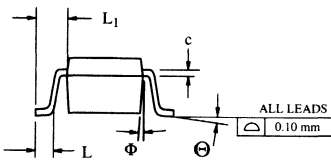
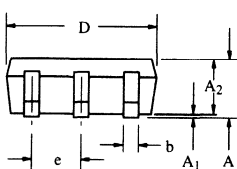
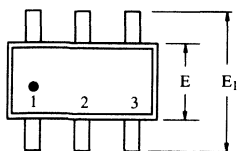
Application Notes for Siliconix Power Products (Cont'd)

Application Note Number	FaxBack Number	Description
Power ICs		
AN707	70580	Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC The Si9120 was designed to get high efficiency from low-power off-line power supplies. This current-mode control PWM IC reduces typical quiescent power requirements to 0.85 mA while driving a 500-pF load at 50 kHz. The chip contains MOS capacitors for the clock circuit, so the only external timing component required is a resistor to set the operating frequency.
AN708	70581	Low-Power Universal-Input Power Supply Achieves High Efficiency A flyback circuit using the Si9120 PWM controller demonstrates that designing universal-input supplies can be a simple task. Good regulation is achieved while maintaining the 3750-V ac input-to-output isolation mandated by VDE. The Si9120 eliminates the need for external start-up circuitry, and its foldback current limiting requires no feedback across the isolation boundary.
AN709	70582	Designing with the Si9976DY N-Channel Half-Bridge Driver and LITTLE FOOT Dual MOSFETs The combination of the Si9976DY and a LITTLE FOOT MOSFET rated between 2 and 5 A creates a powerful and flexible solution for power switching in dc motor drives in 20- to 40-V systems.
AN710	70583	High-Efficiency Buck Converter for Notebook Computers This application note presents a dc-to-dc converter consisting of the Si9150CY BiCMOS controller IC and LITTLE FOOT low-voltage MOSFETs. In notebook computers and other portable products, the converter achieves a maximum efficiency of 94% while producing 400 mA at 3.3 V with input voltage of 6 V. The low losses of this efficient buck converter eliminate the need for heavy heat sinks and device packaging, and makes energy that is normally consumed by the power converter available for the application.
AN713	70584	A 1-Watt Flyback Converter Using the Si9100 Power integrated circuit technology allows low-power CMOS control circuits to be combined with DMOS power transistors in the Si9100. The resulting reduction in parts count decreases system cost, improves reliability, and simplifies circuit design in feature phones and ISDN terminals.
AN714	70585	A Compact Controller for Brushless DC Motors The Si9979 is a monolithic controller with integral high-side drive circuitry, allowing easy implementation of an all-n-channel three-phase bridge. An internal voltage regulator allows the Si9979 to operate over a wide input voltage range, 20 to 40 V DC, and to power commutation sensors over this same range. Housed in a 7 mm SQFP package, the Si9979 reduces assembly cost and simplifies both motor and electronics packaging.
AN715	70586	Designing Low-Voltage DC/DC Converters with the Si9145 The Si9145 switchmode controller IC is designed to make dc-to-dc conversion smaller and more efficient in low-voltage, low-power applications such as portable cellular phones and other battery-operated equipment. This small-outline device has been configured so that the most popular conventional topologies, including buck, synchronous buck, and boost can be easily implemented.
AN716	70587	Designing with Siliconix PC Card (PCMCIA) Power Interface Switches Siliconix offers a series of integrated power MOSFETs specifically designed for the strict demands of the PC Card power interface. The Si97XX series includes devices supporting one and two PC Card slots in battery-operated notebook, subnotebook, and palmtop computers.
AN718	70588	Powering the Pentium™ VRE with the Si9145 Voltage Mode Controlled PWM Converter Built on a leading-edge CBiC/D process, Siliconix' Si9145BY is the only voltage-mode controlled PWM IC capable of switching up to 2 MHz and providing a 25-MHz error amplifier. Its 100-kHz closed-loop bandwidth switching converter meets the dynamic switching transient requirements of the Pentium microprocessor without the need for numerous output capacitors.
AN719	70589	Using the Si9145 PWM Converter with the Pentium™ P55 and P6 Microprocessors Although the P55 and P6 Pentium microprocessors push the limits of switching power supplies, the Si9145 PWM controller IC meets their demanding requirements with switching speeds of 400 kHz and a 25-MHz error amplifier to generate a 100-kHz closed-loop converter bandwidth.
AN720	70590	Si9986CY Buffered H-Bridge The Si9986CY is a buffered H-bridge that will eliminate all the external discretes that are normally needed to prevent shoot-through in low-voltage brushed motor, stepper motor, and actuator applications.

Application Notes for Siliconix Power Products (Cont'd)

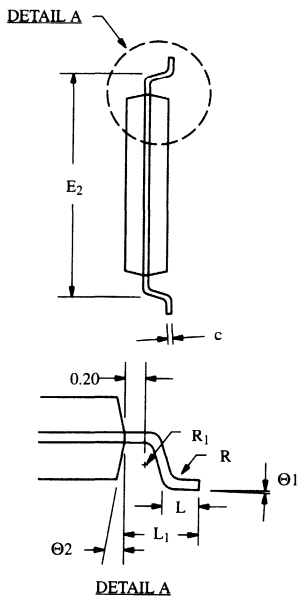
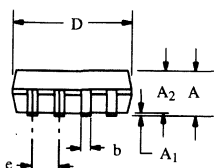
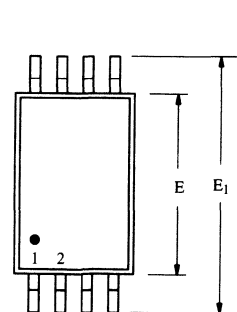
Application Note Number	FaxBack Number	Description
Power ICs		
AN721	70710	An Elementary Introduction to Power Supply Specifications This application note is intended for those who specify power supplies and for novice designers, who have almost no previous experience with power supplies and their specifications. It briefly outlines some of the key terms in specifying power supplies and gives some general guidelines relevant to understanding modern supplies.
AN722	70733	An Introduction to Power Supplies and Controller ICs This application note is intended for those who specify power supplies and for novice designers, who have a level of previous experience with power supplies and their specifications equivalent to that given by the application note "An Elementary Introduction to Power Supply Specifications." It discusses some of the key terms in specifying power supplies in greater detail than that application note, and gives more detailed information on what parameters of controller ICs determine the performance of modern switching power supplies.

TSOP: 6 Leads



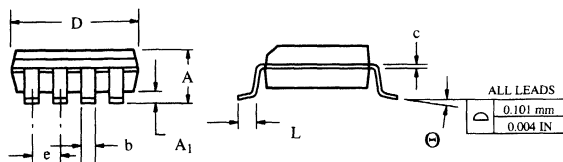
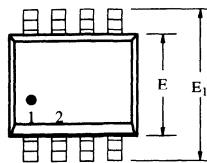
Dim	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.91	—	1.10	0.036	—	0.043
A ₁	0.01	—	0.10	0.0004	—	0.004
A ₂	0.80	—	1.00	0.031	—	0.039
b	0.25	0.32	0.50	0.010	0.013	0.020
c	0.10	0.15	0.26	0.004	0.006	0.010
D	2.90	3.05	3.10	0.114	0.120	0.122
E	1.30	1.65	1.70	0.051	0.065	0.067
E ₁	2.70	2.85	2.98	0.106	0.112	0.117
e	1.00 BSC			0.0394 BSC		
L	0.20	0.33	0.60	0.008	0.013	0.024
L ₁	—	0.64	—	—	0.25	—
Θ	0°	—	8°	0°	—	8°
Φ	7° NOM			7° NOM		

TSSOP: 8 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.05	1.20	0.041	0.047
A ₁	0.05	0.15	0.002	0.006
A ₂	0.80	1.05	0.032	0.041
b	0.19	0.30	0.008	0.012
c	0.127 NOM		0.005 NOM	
D	2.90	3.10	0.114	0.122
E	4.30	4.50	0.170	0.177
E ₁	6.20	6.60	0.240	0.260
E ₂	5.14	5.24	0.202	0.206
e	0.65 BSC		0.025 BSC	
L	0.45	0.75	0.018	0.030
L ₁	0.90	1.10	0.355	0.433
R	0.09	—	0.004	—
R ₁	0.09	—	0.004	—
Θ ₁	0°	8°	0°	8°
Θ ₂	12°			

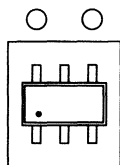
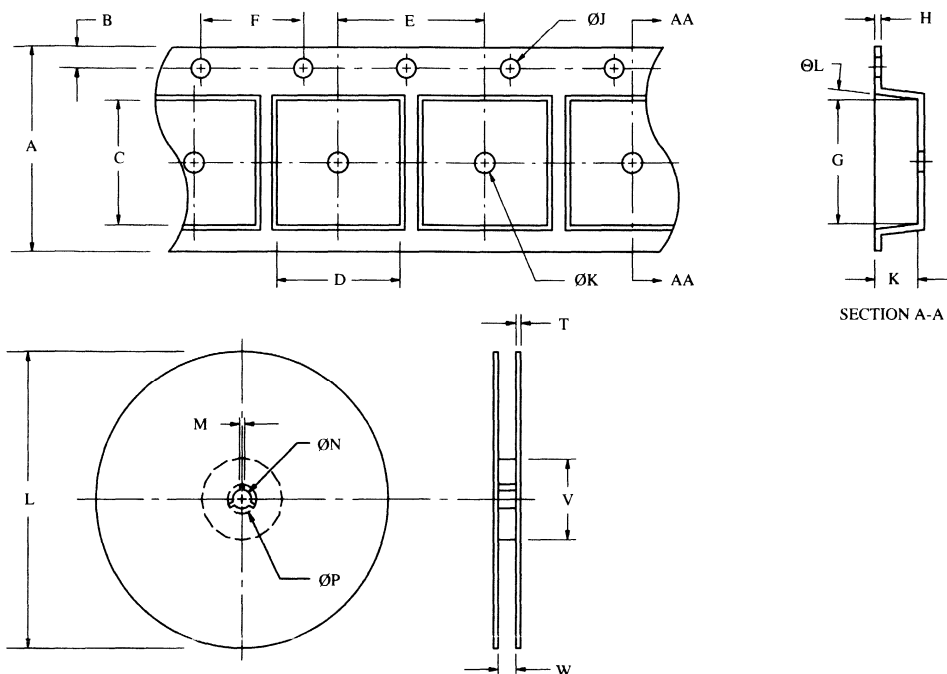
SOIC: 8 Leads



Note: Pin 1 may be designated by a dot or chamfered edge.

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
D-8	4.80	5.00	0.189	0.197
E	3.80	4.00	0.149	0.157
E ₁	5.80	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050
Θ	0°	8°	0°	8°

Tape and Reel Options for TSOP-6

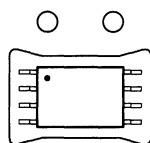
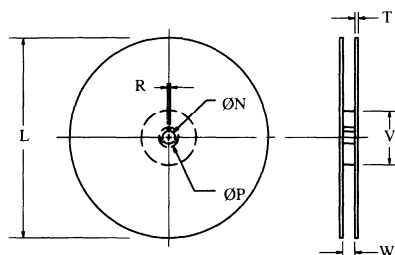
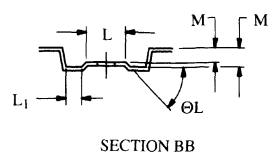
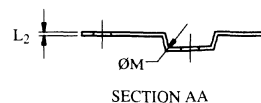
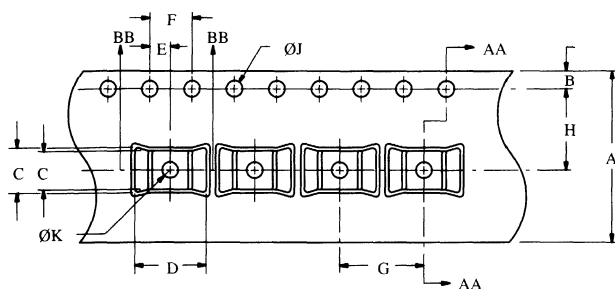


Package Orientation

Quantity Per Reel		
Device	Size	Quantity
Si34xxDX-T1	7-inches	3,000
Si34xxDX-T2	7-inches	500
Si34xxDX-T3	13-inches	10,000

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	7.70	8.30	0.303	0.327
B	1.65	1.85	0.065	0.073
C	3.10	3.30	0.122	0.130
D	3.05	3.25	0.120	0.128
E	3.90	4.10	0.154	0.161
F	3.90	4.10	0.154	0.161
G	3.10	3.30	0.122	0.130
H	0.17	0.23	0.007	0.009
ØJ	1.50	1.60	0.059	0.063
K	1.30	1.50	0.051	0.059
ØK	1.00	1.10	0.039	0.043
L (T1, 2)	170	180	6.929	7.087
L (T3)	328	332	12.91	13.07
ØL	—	3°	—	3°
M	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.846	0.886
T	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126
W	7.90	8.90	0.311	0.350

Tape and Reel Options for TSSOP-8

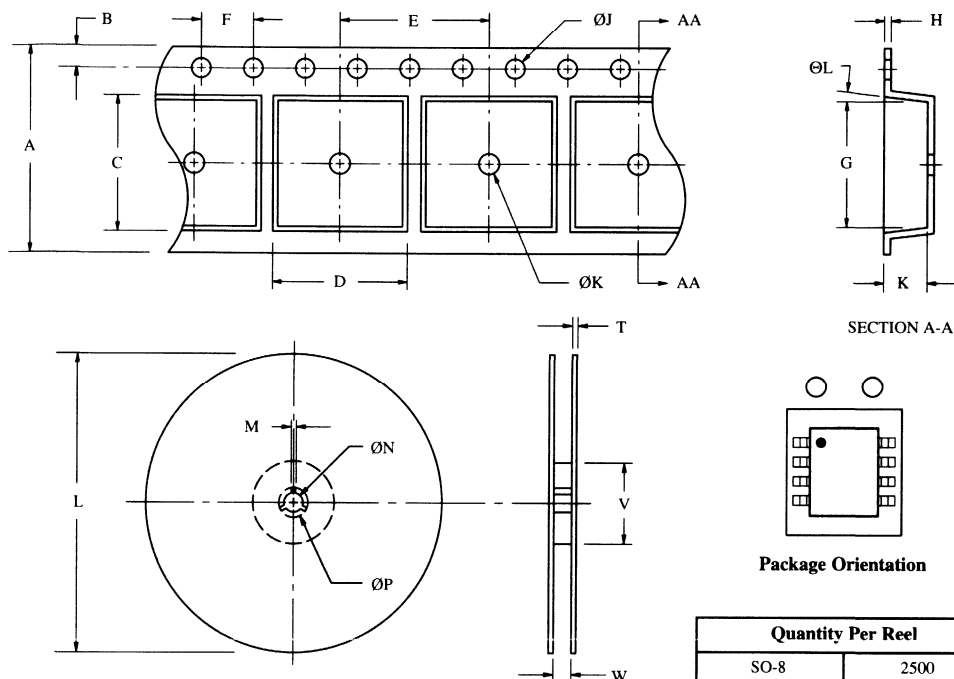


Package Orientation

Quantity Per Reel	
TSSOP-8	3000

Dim	TSSOP-8			
	Millimeters		Inches	
	Min	Max	Min	Max
A	15.70	16.30	0.618	0.641
B	1.65	1.85	0.065	0.073
C	3.50	3.70	0.138	0.146
C ₁	4.20	4.40	0.165	0.173
D	6.80	7.00	0.268	0.276
E	1.95	2.05	0.076	0.080
F	3.90	4.10	0.154	0.161
G	7.90	8.10	0.311	0.319
H	7.40	7.60	0.291	0.299
ØJ	1.50	1.60	0.059	0.063
ØK	1.50	1.60	0.059	0.063
L	3.30	3.5	0.130	0.138
L ₁	1.27	1.47	0.050	0.058
L ₂	0.25	0.35	0.010	0.014
ØL	—	45°	—	450
M	1.10	1.30	0.043	0.051
M ₁	1.50	1.70	0.059	0.067
ØM	—	0.30	—	0.013
R	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126
W	16.4	18.4	0.646	0.724

Tape and Reel Options for SO-8



Dim	SO-8			
	Millimeters		Inches	
	Min	Max	Min	Max
A	11.9	12.1	0.469	0.476
B	1.65	1.85	0.065	0.073
C	5.10	5.30	0.201	0.209
D	6.30	6.50	0.248	0.256
E	7.90	8.60	0.311	0.339
F	3.90	4.10	0.154	0.161
G	5.10	5.30	0.200	0.209
H	0.25	0.35	0.010	0.014
ØJ	1.50	1.60	0.059	0.063
K	1.90	2.30	0.075	0.091
ØK	1.50	1.70	0.059	0.067
L	328	332	12.91	13.07
ØL	-	3°	-	3°
M	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126
W	12.4	14.4	0.488	2.667

Selector Guides	
TSOP-6	
TSSOP-8	
SOIC-8	
Application Specific Standard MOSFETs (ASSM)	
Appendix	
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